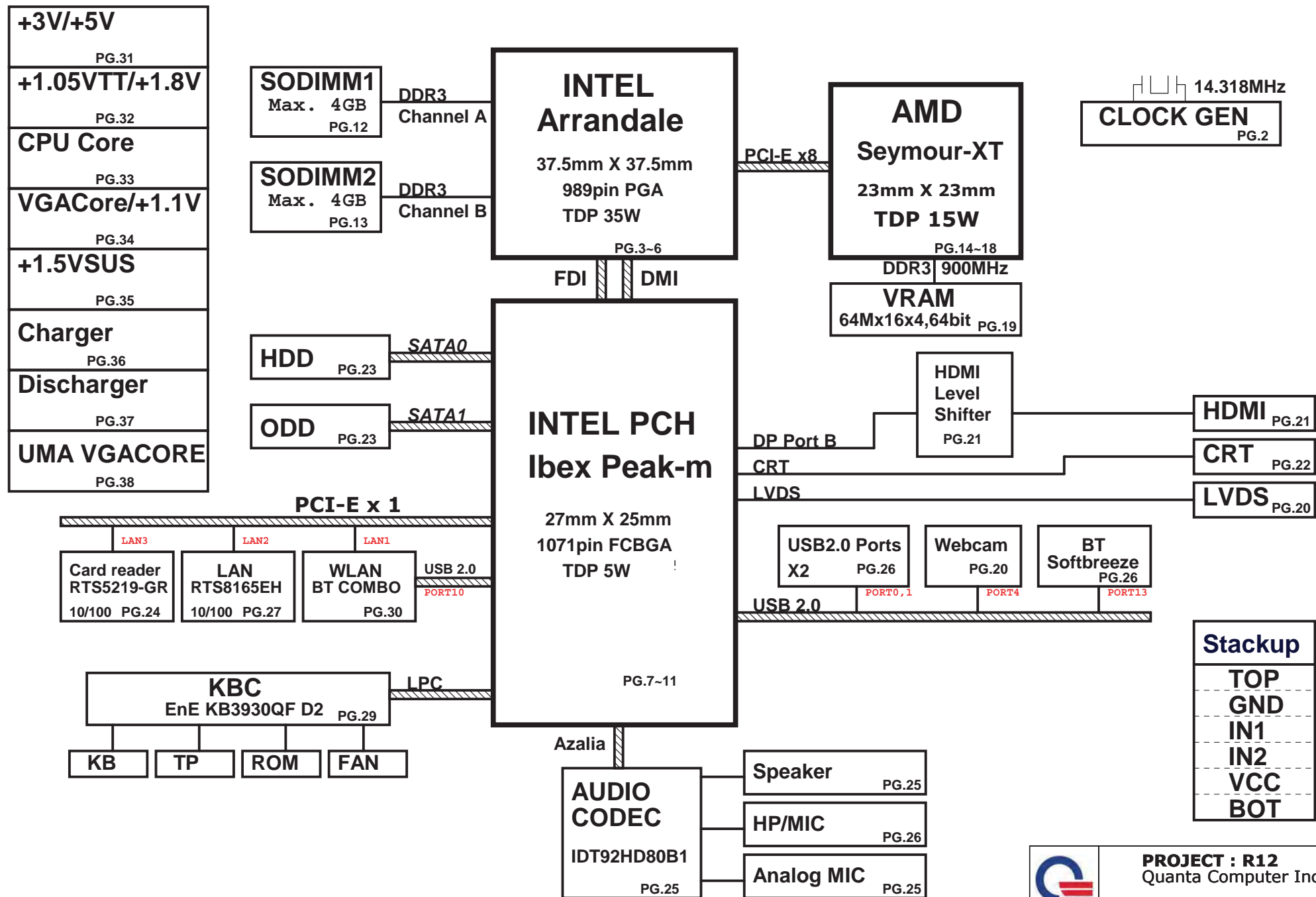
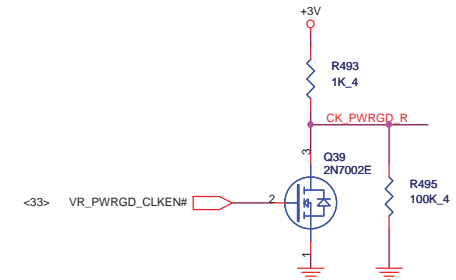
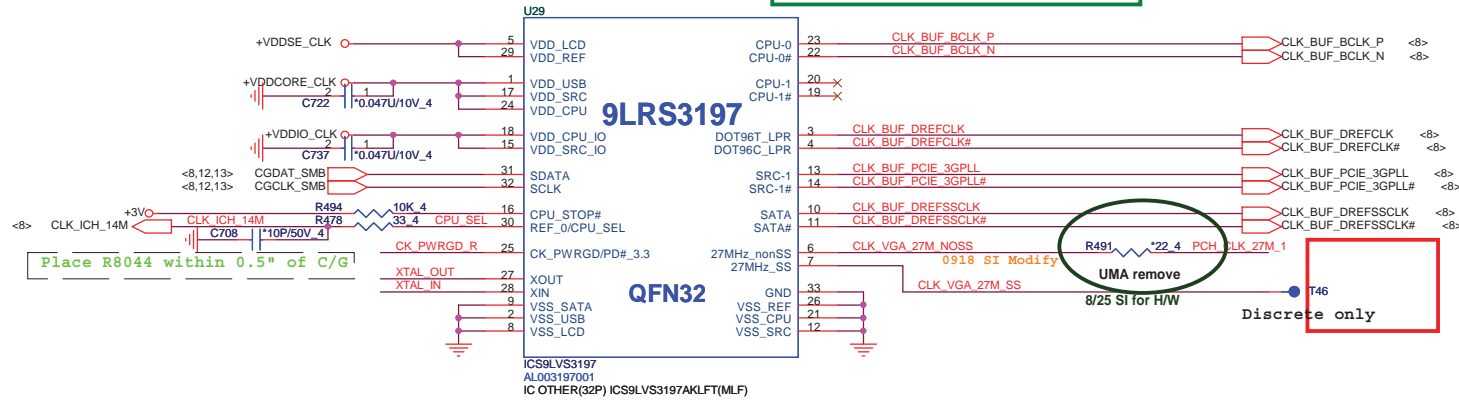
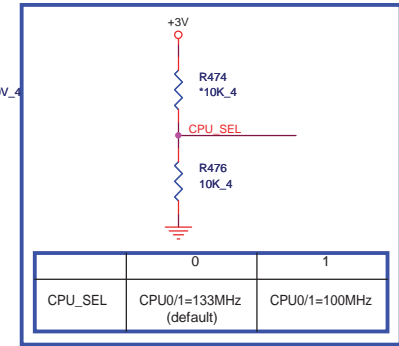
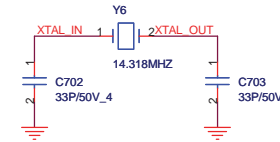
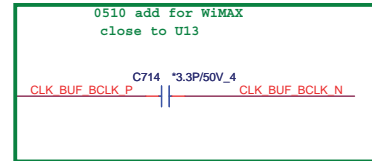
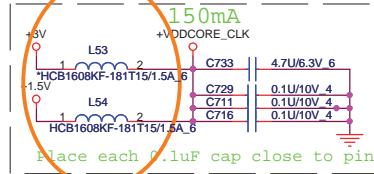
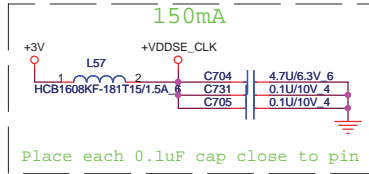
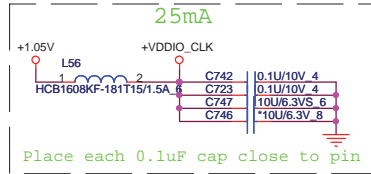
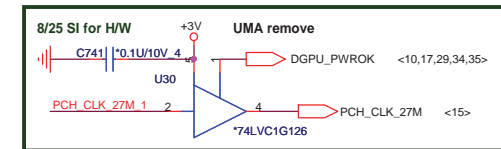


# R12 INTEL UMA/DISCRETE SYSTEM DIAGRAM





Vender	Part	Part Number	Part Description
ICS	ICS9LV3197	AL003197000	IC OTHER(32P) ICS9LV3197AKLFT(MLF)
Realtek	RTM890N-632	AL000890000	IC OTHER(32P) RTM890N-632-GRT(QFN)
Silego	SLG8LV595VTR	AL000595000	IC OTHER(32P)SLG8LV595VTR(QFN)



+1.05V <7,8,9,11,39>

+1.5V <5,30>

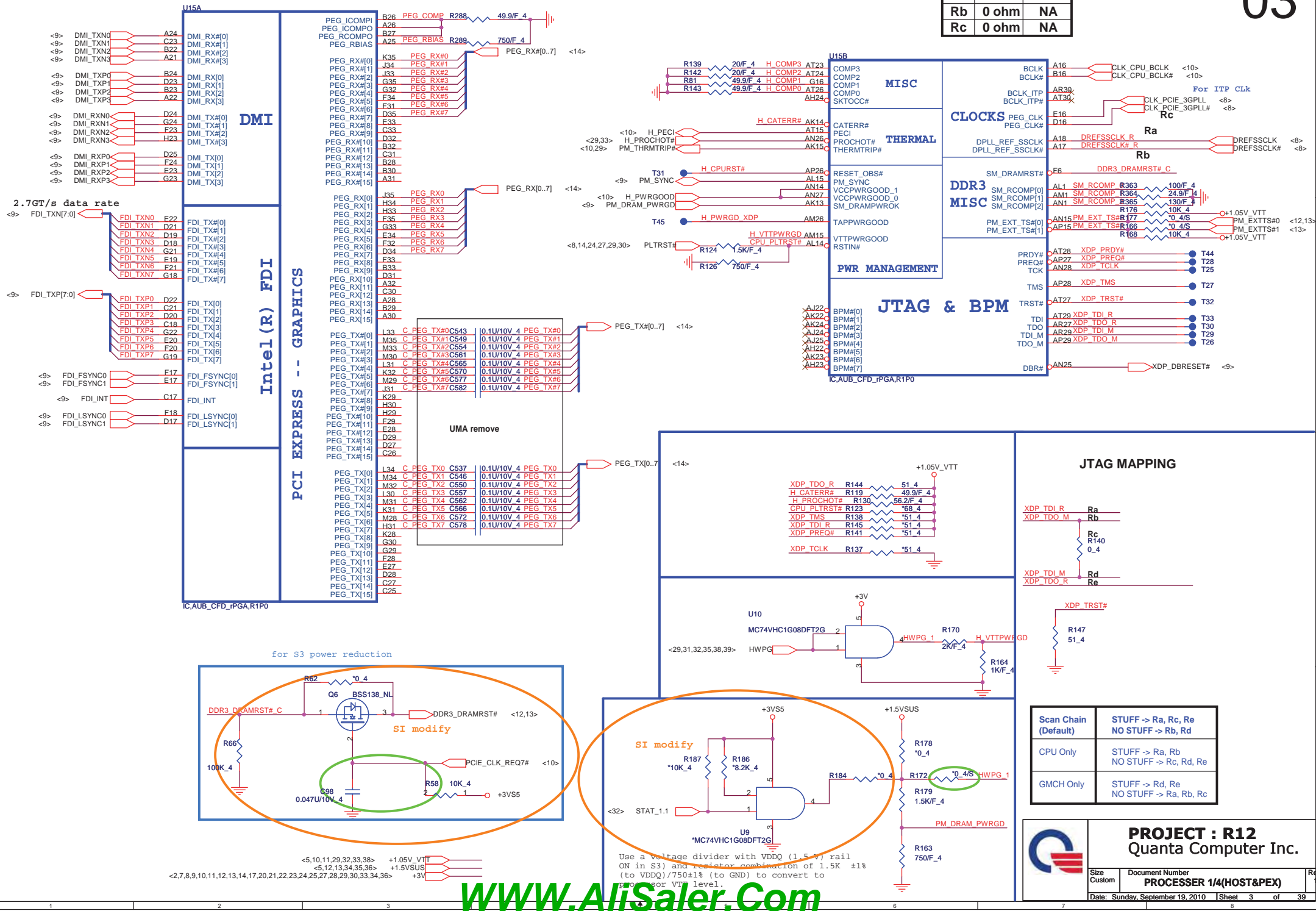
+3V <3,7,8,9,10,11,12,13,14,17,20,21,22,23,24,25,27,28,29,30,33,34,36>



**PROJECT : R12**  
Quanta Computer Inc.

Size Custom	Document Number Clock Gen(9LRS3197)	Rev 1A
Date: Sunday, September 19, 2010	Sheet 2 of 39	

	DIS	UMA
Ra	NA	0 ohm
Rb	0 ohm	NA
Rc	0 ohm	NA

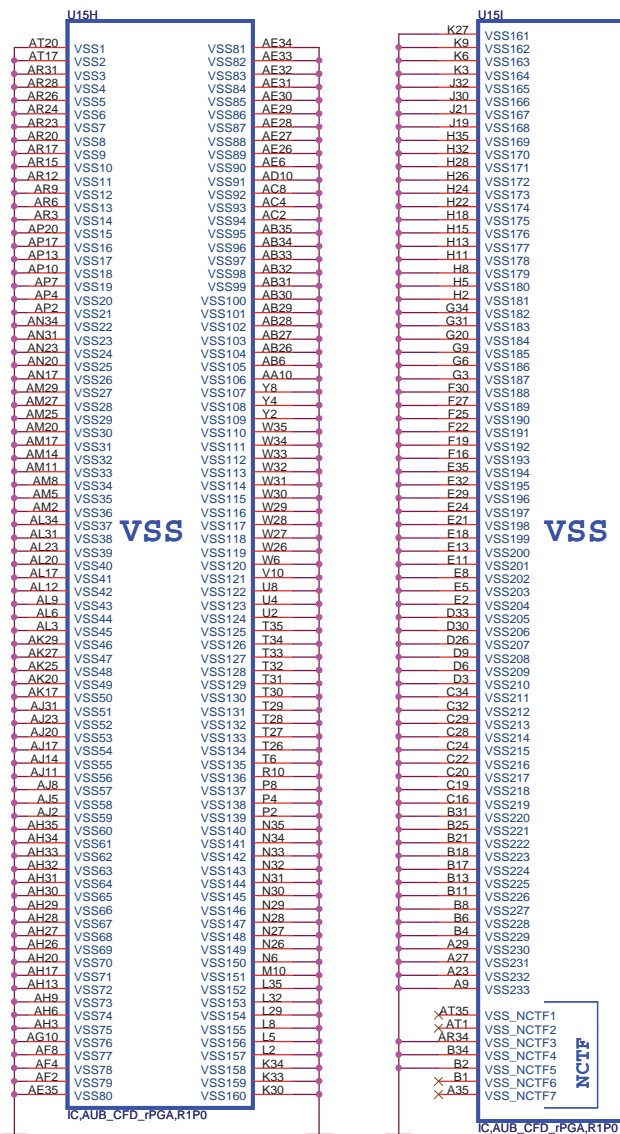


[illegible]



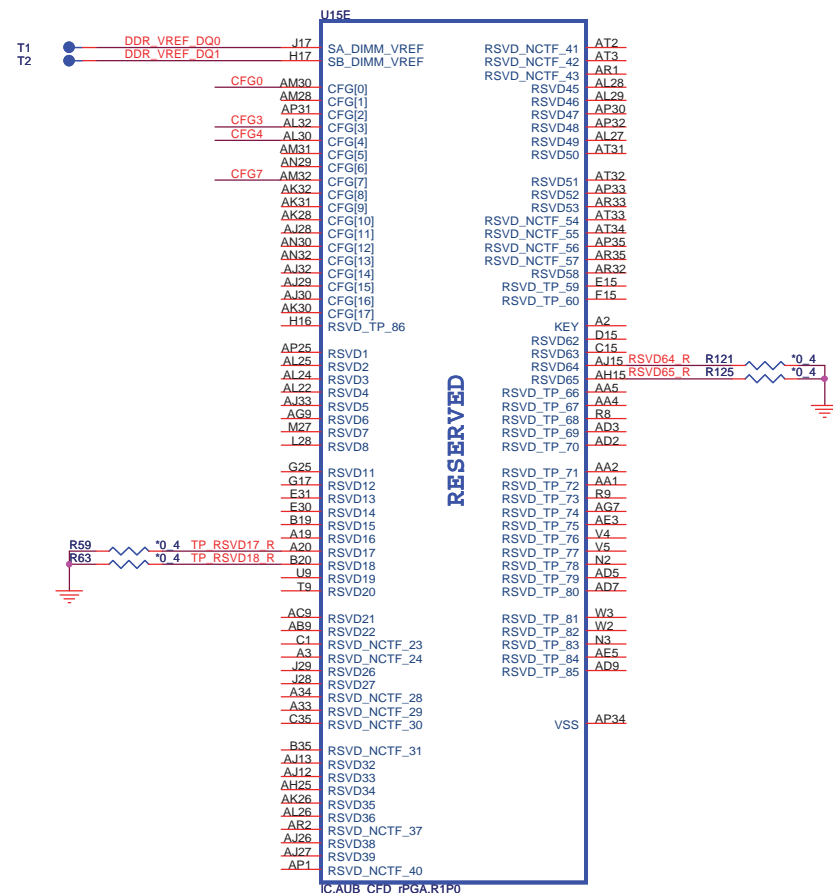


## AUBURNDALE/CLARKSFIELD PROCESSOR (GND)



The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01k  $\pm$  5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

**AUBURNDALE/CLARKSFIELD PROCESSOR( RESERVED, CFG)**



For Discrete only



```
CFG[ 1:0 ] - PCI_Epress Configuration Select
* 11= 1 x 16 PEG
* 10= 2 x 8 PEG
```

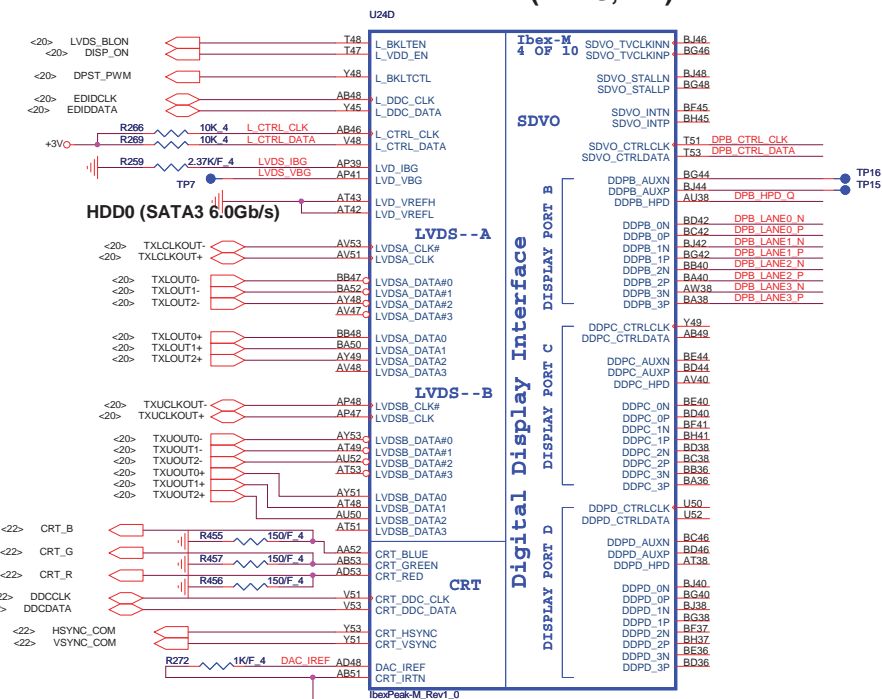


**PROJECT : R12**  
Quanta Computer Inc.

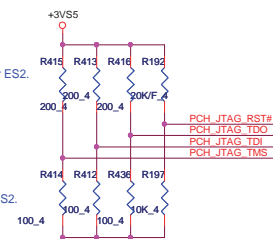
Size Custom	Document Number <b>PROCESSER 4/4 (GND)</b>	Rev 1A
Date: Sunday, September 19, 2010		Sheet 6 of 39

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed 15 -> 0 , 14 -> 1

### IBEX PEAK-M (LVDS,DDI)

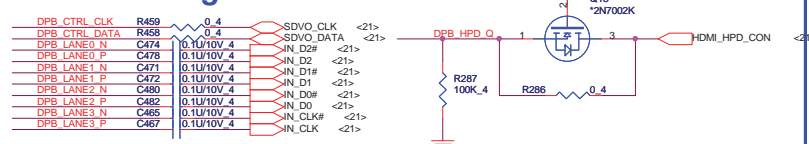


1 requires a  
1-up (8.2 k  
3.

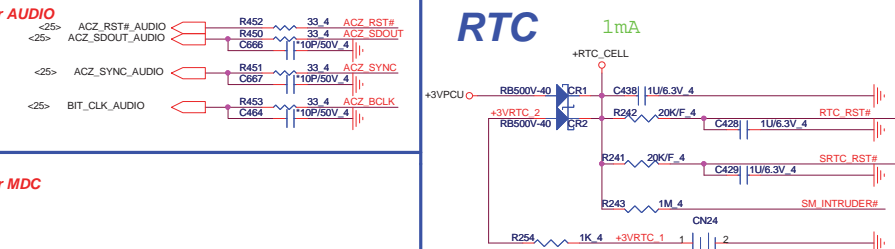


Part	Part Number	Part Description
------	-------------	------------------

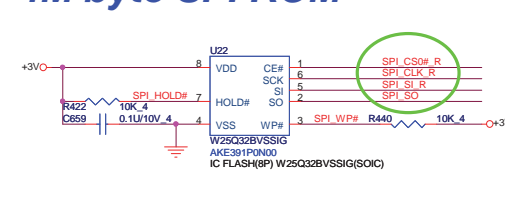
For ES1 ONLY, NI for ES2.



**RTC**



### 4M byte SPI ROM



Socket DG008000031

AKF39FN0000 IC FLASH(8P) EN25F32-100HIP (SOIC

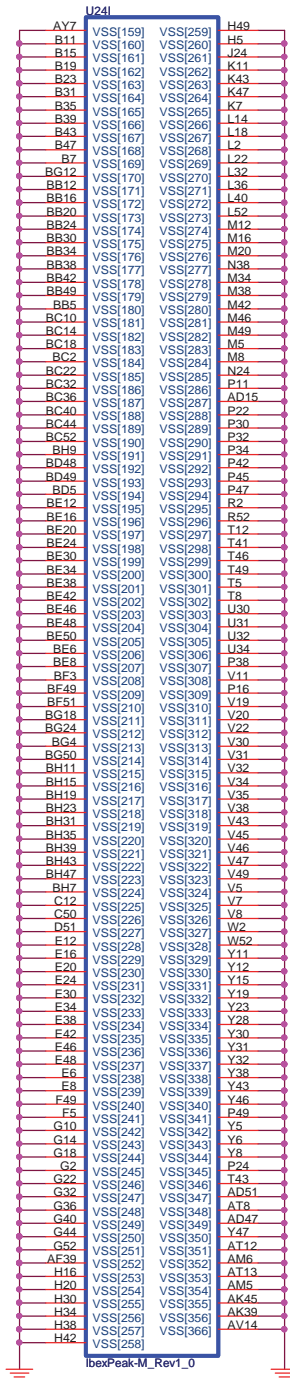
AKE391P0N00 IC FLASH(8P) W25Q32BVSSIG(SOIC)

ARESTH ONSS TO FLEASH(OF) WZSQSZDVCCIC(COIC)

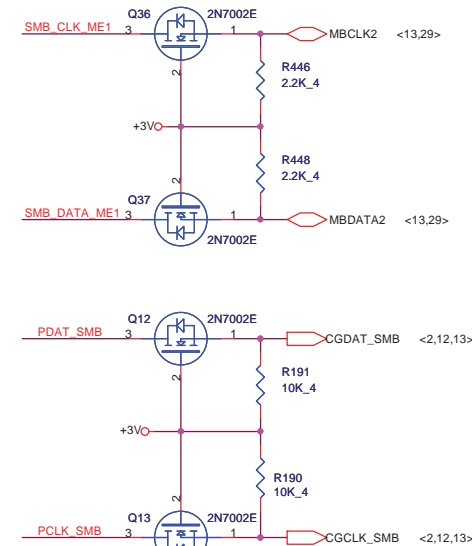
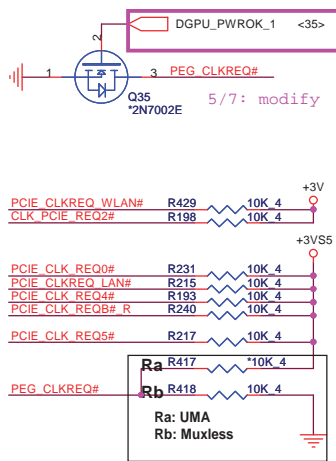


**PROJECT : R12**  
Quanta Computer Inc.

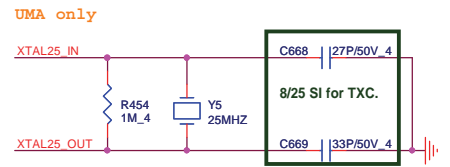
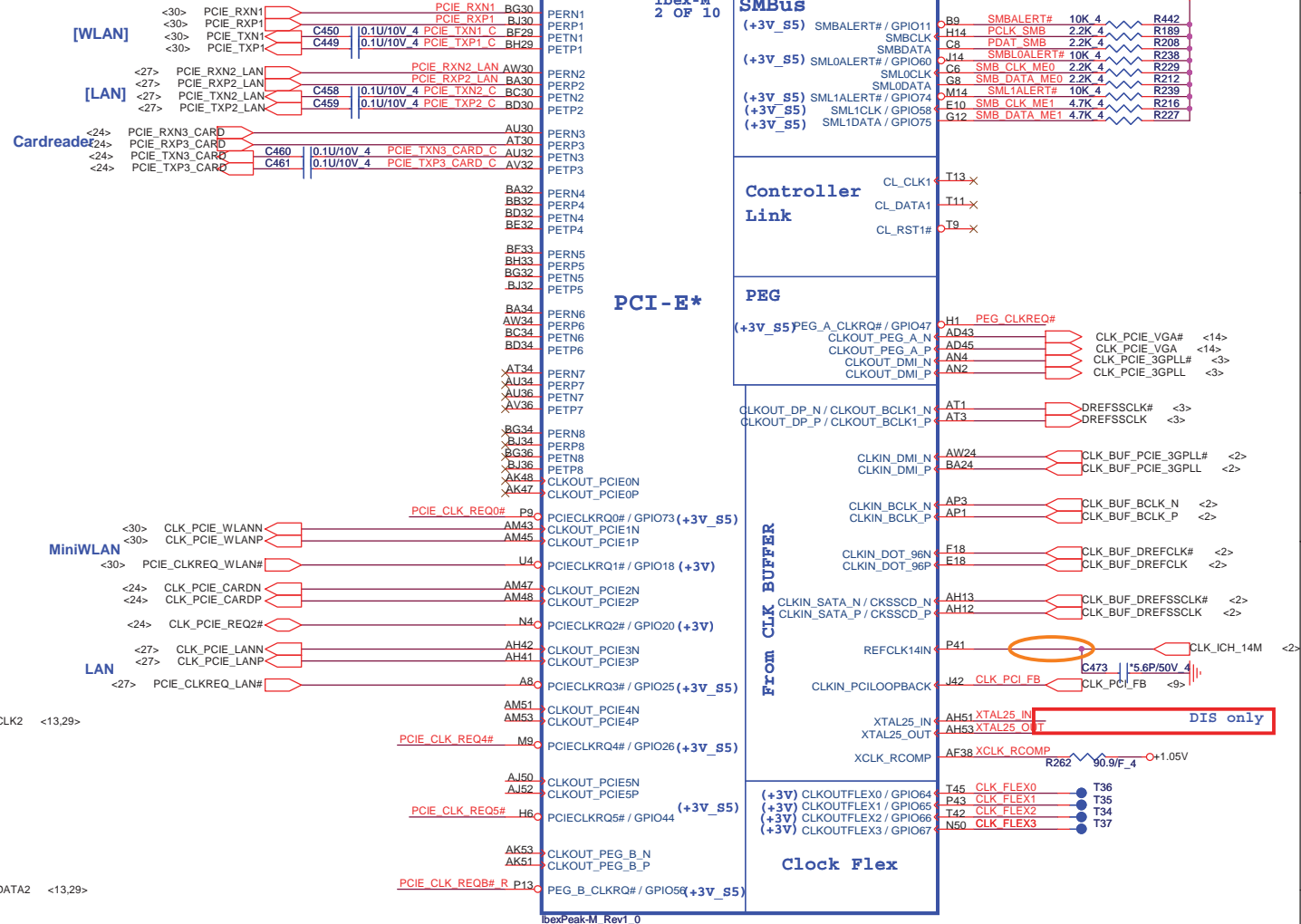
Size Custom	Document Number <b>PCH 1/5 (SATA,HDA,LPC)</b>	Rev 1
Date: Sunday, September 19, 2010	Sheet 7 of 39	



### PEG Clock detect (SG only)

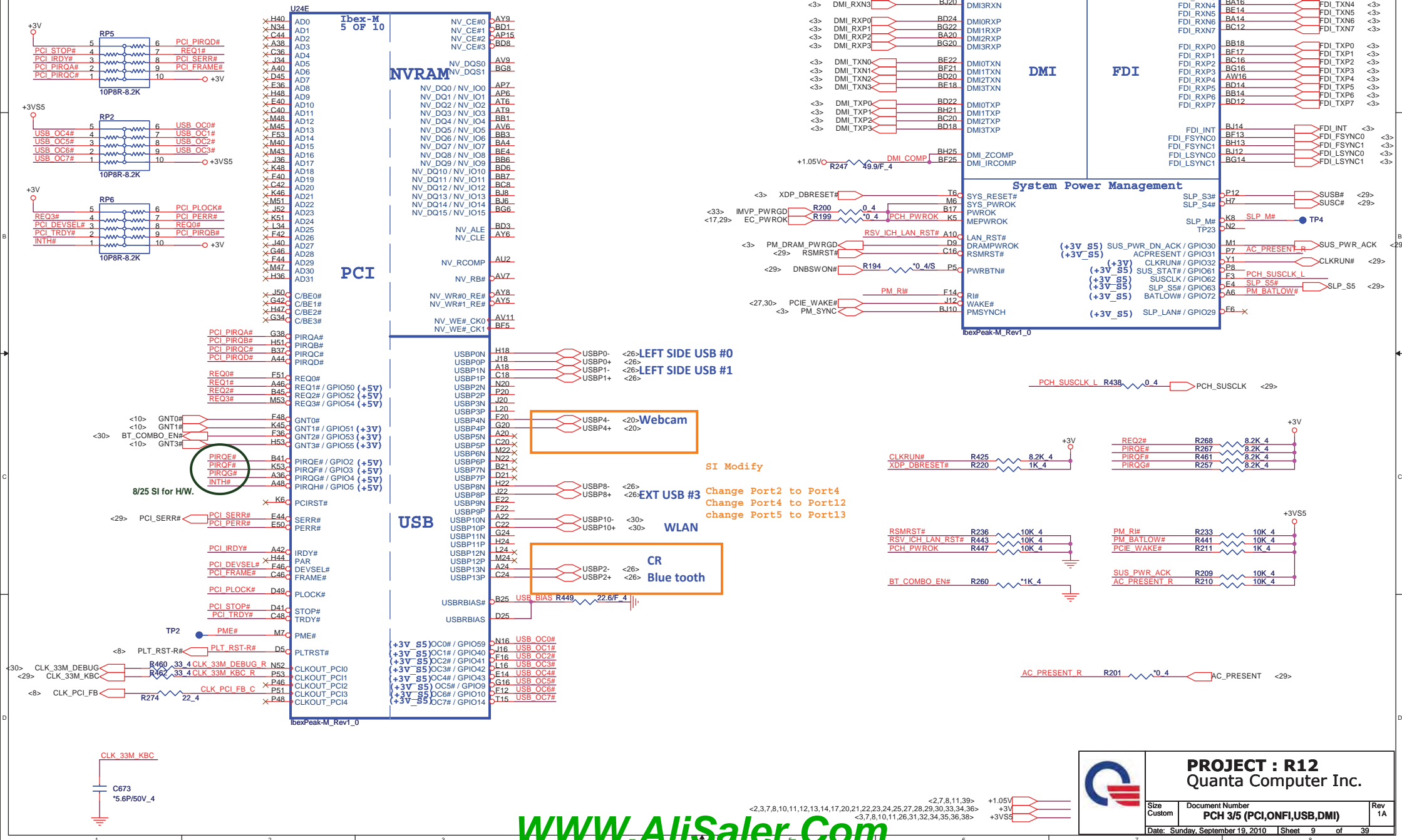


### IBEX PEAK-M (PCI-E, SMBUS, CLK)



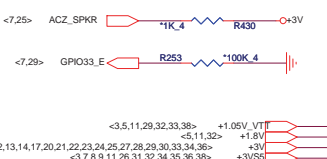
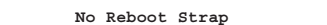
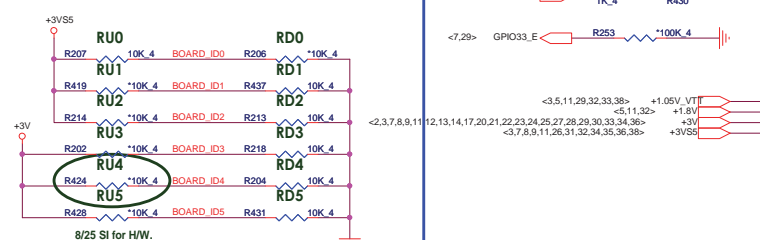


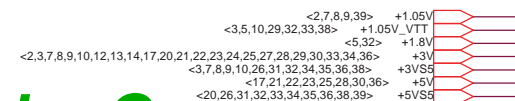
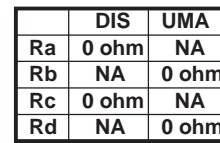
## IBEX PEAK-M (DMI,FDI,GPIO)

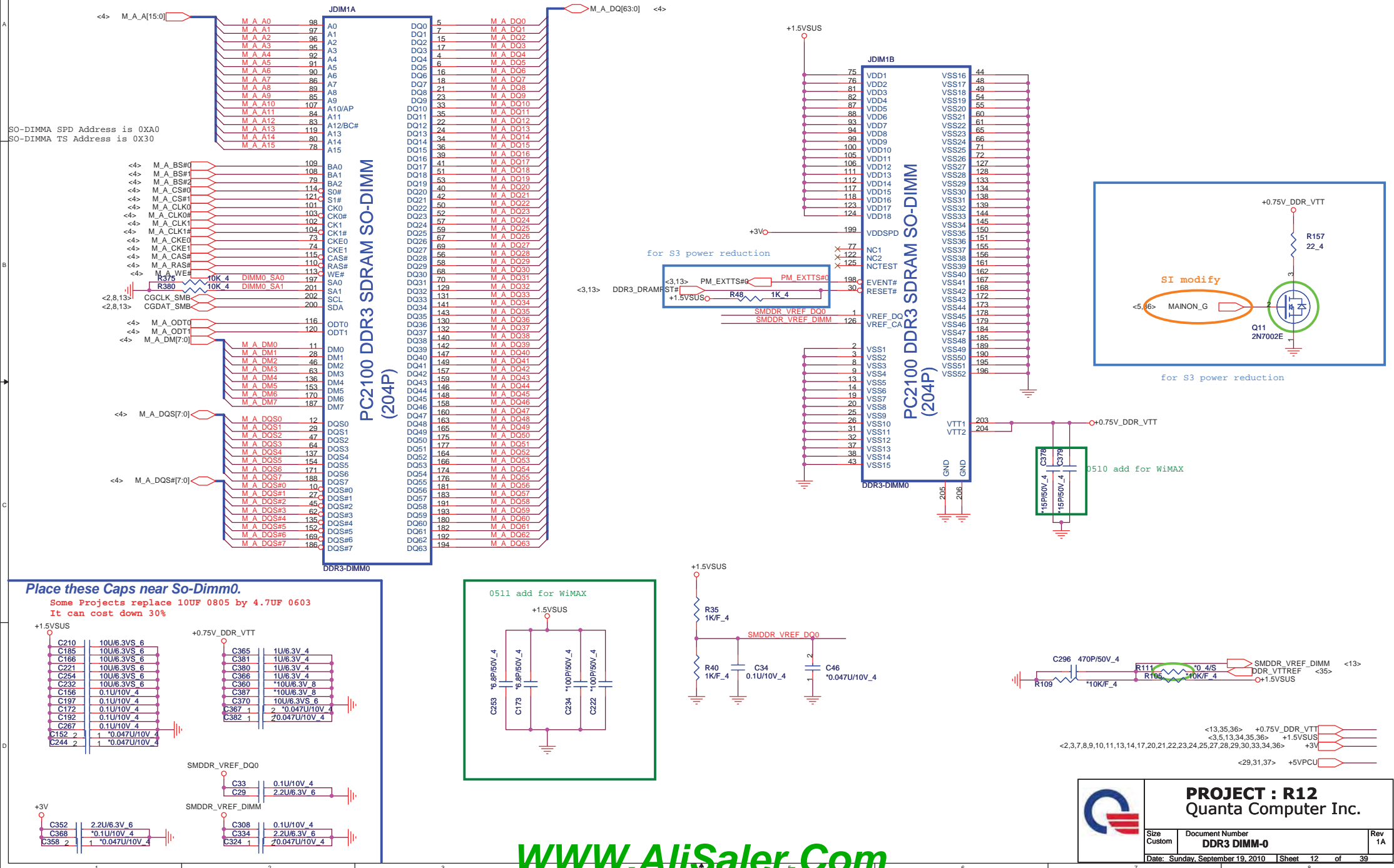




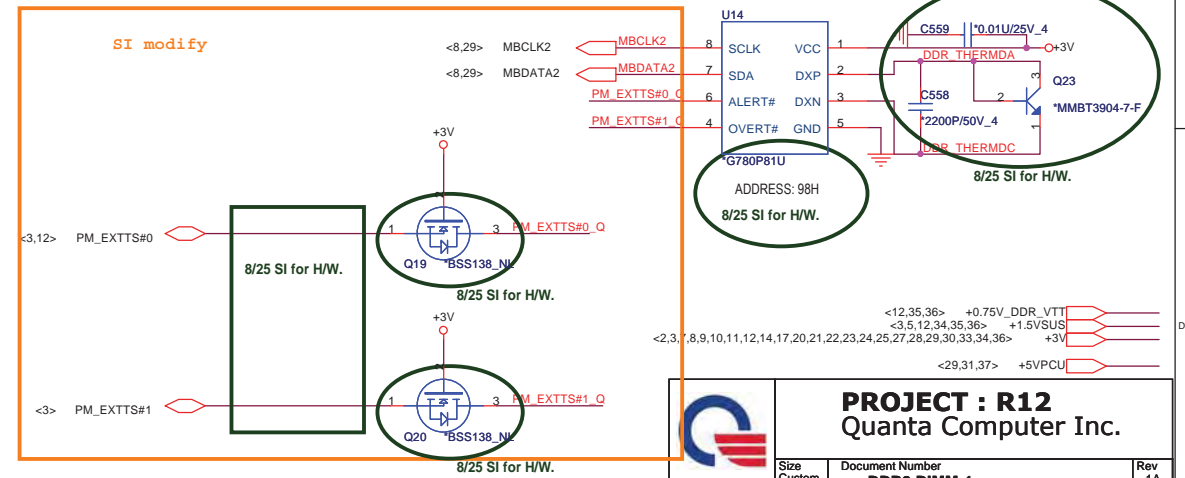
Board ID	ID0 GPIO24	ID1 GPIO45	ID2 GPIO57	ID3 GPIO34	ID4 GPIO35	ID5 GPIO38
UMA/DIS	0=UMA 1=DIS.					
Reserve		0=No 1=Yes				
Reserve			0=No 1=Yes			
Reserve				0=No 1=Yes		
Reserve					0=No 1=Yes	
Reserve						0=No 1=Yes



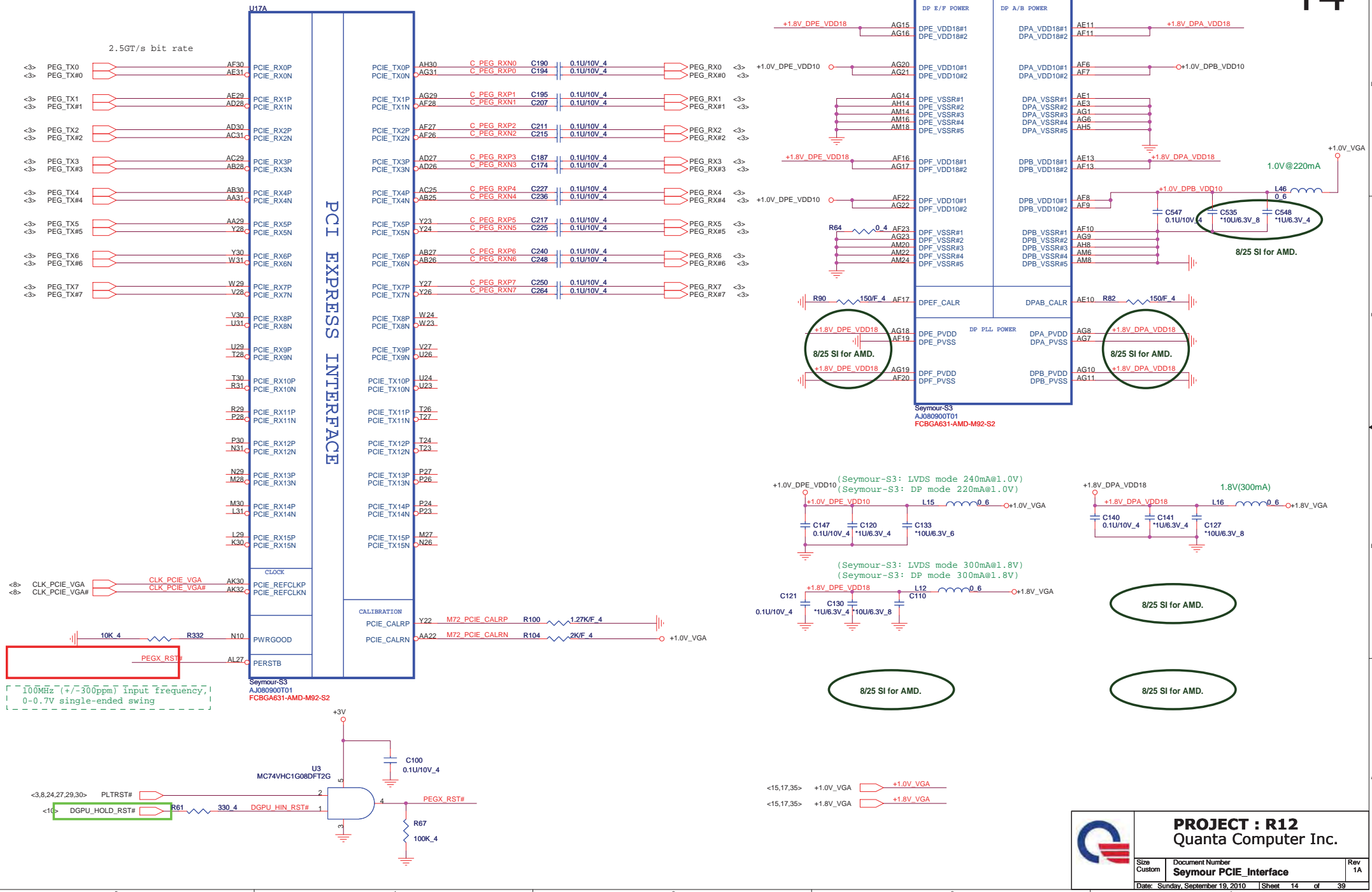




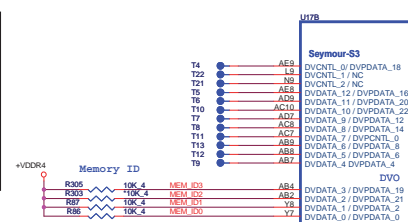


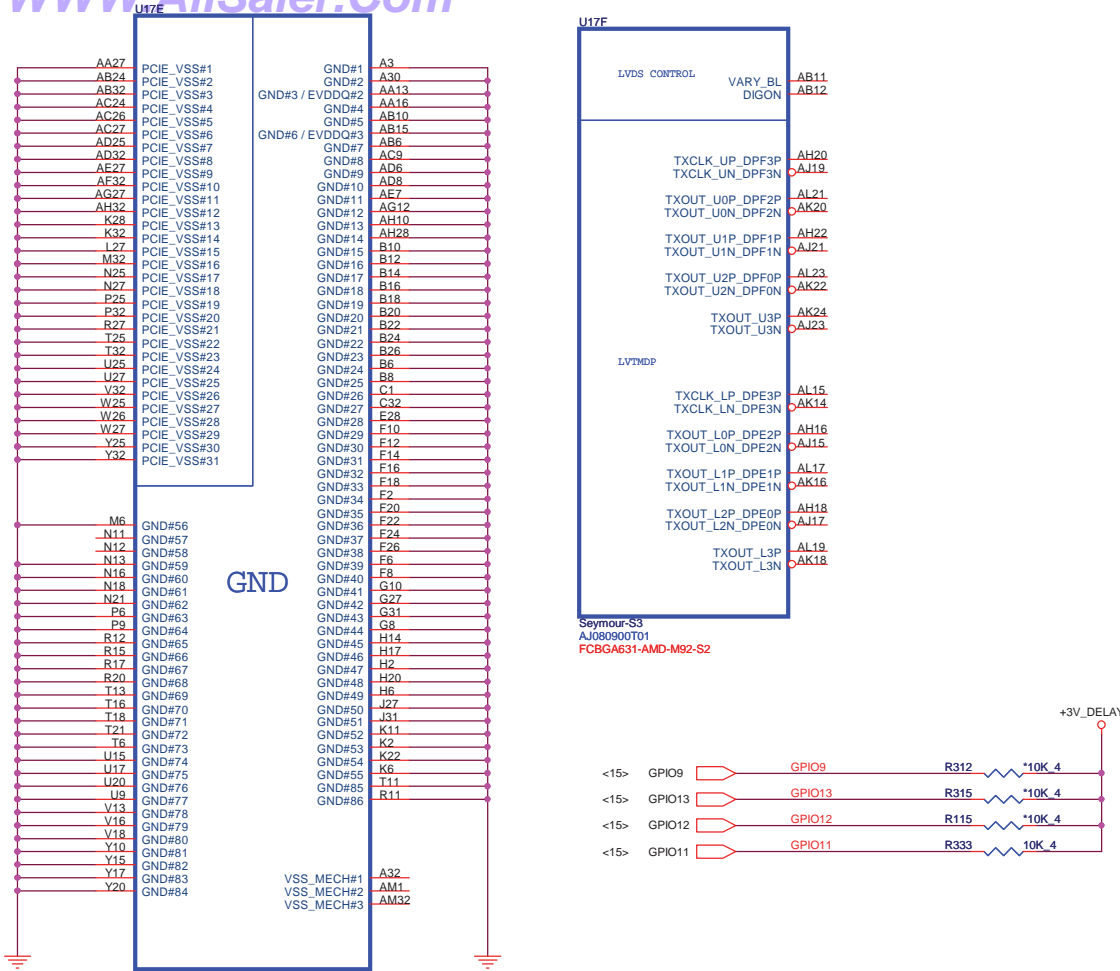




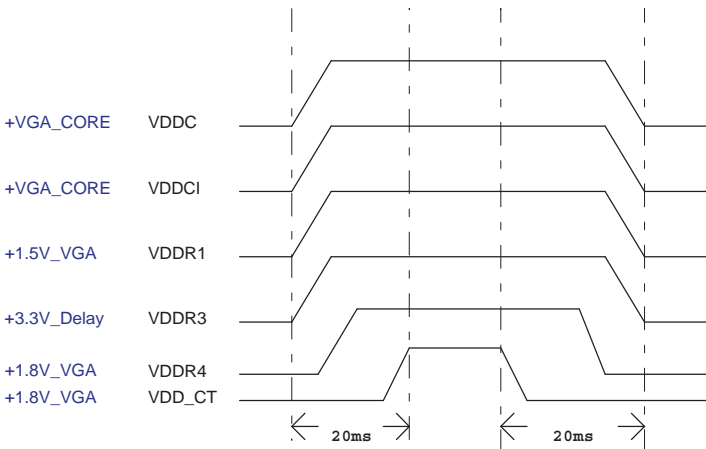


MEM_ID[3:0]	Vendor	Type	Vendor P/N
0000	Samsung- E die	64*16-900MHZ	K4W1G1646G-BC12
0001	Hynix- Vega die	64*16-800MHZ	H5TQ1G63DFR-12C
0010	Hynix- Vega die	128*16-800MHZ	H5TQ1G63DFR-12C
0011	Samsung- C die	128*16-800MHZ	K4W2G1646G-BC12
0100	Micro	128*16-800MHZ	MT47A128M16DA-125:D
0101			Reserved
0110	Hynix- Vega die	64*16-900MHZ	H5TQ1G63DFR-11C
0111	Samsung- E die	64*16-900MHZ	K4W1G1646G-BC11
1000	Samsung- G die	64*16-900MHZ	K4W1G1646G-BC11
1001			Reserved
1010	Hynix- Vega die	128*16-900MHZ	H5TQ2G63DFR-11C
1011	Samsung- E die	128*16-900MHZ	K4W2G1646G-BC11
1100			Reserved
1101			Reserved
1110			Reserved
1111			Reserved





Power Up/Down Sequence



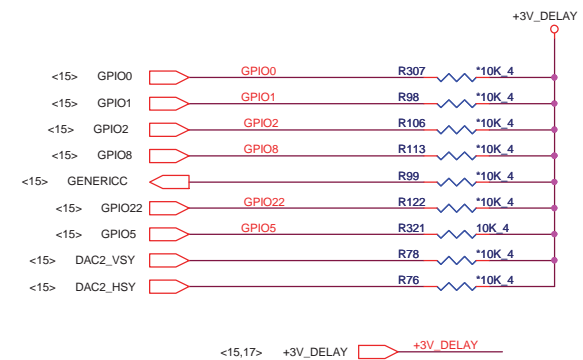
Memory Aperture size

GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS\_ROM\_EN is set to 0.

CONFIGURATION STRAPS			RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1= INSTALL 10K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET			
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	<b>Transmitter Power Savings Enable</b> 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	<b>PCI Express Transmitter De-emphasis Enable</b> 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN_A	GPIO2	<b>Enable CLKREQ# Power Management</b> 0 - CLKREQ# power management capability is disabled 1 - CLKREQ# power management capability is enabled	0
RSVD BIF_VGA_DIS RSVD	GPIO8 GPIO9 GPIO21	VGA ENABLED	0 0 0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD AUD[1] AUD[0]	GENERICC HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	0 0 11

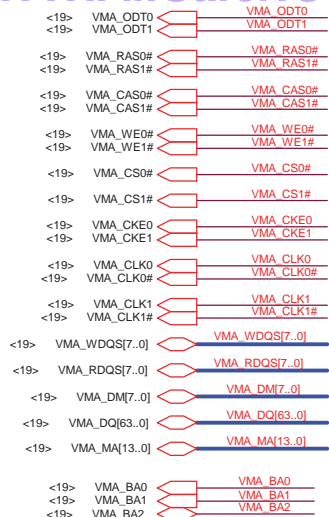
AMD RESERVED CONFIGURATION STRAPS		
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET		
H2SYNC	GENERICC	
PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET		
GPIO21_BB_EN		



**PROJECT : R12**  
Quanta Computer Inc.

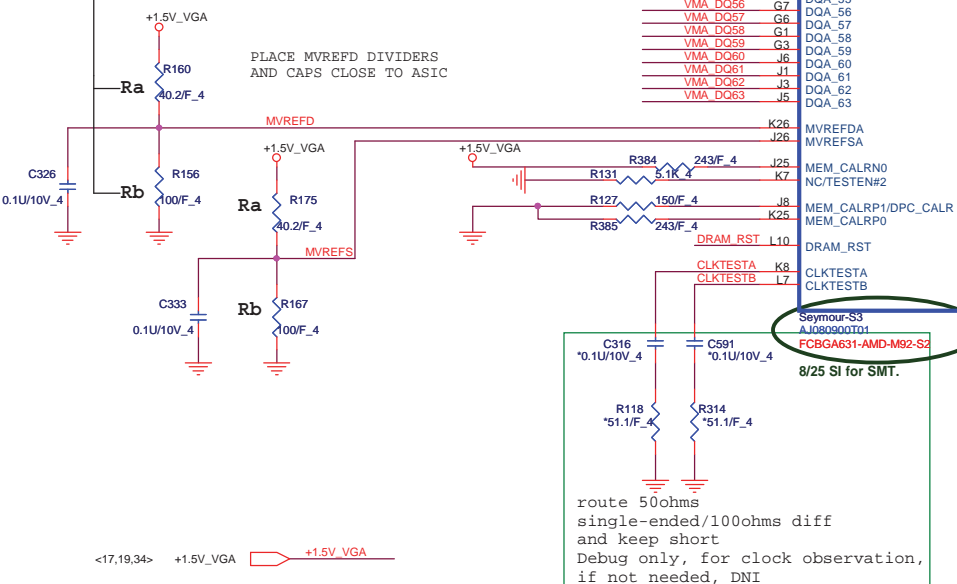
Size Custom	Document Number <b>Seymour GND / LVDS/ Straps</b>	Rev 1A
Date: Sunday, September 19, 2010	Sheet 16 of 39	



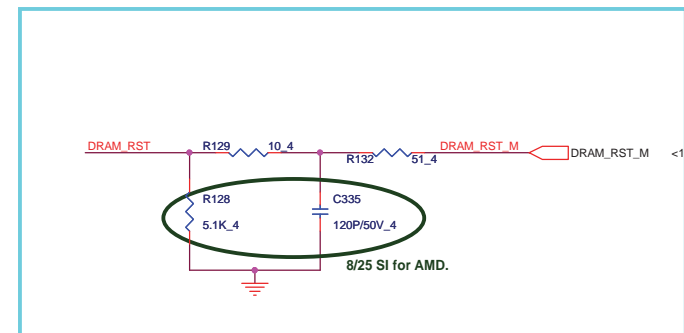
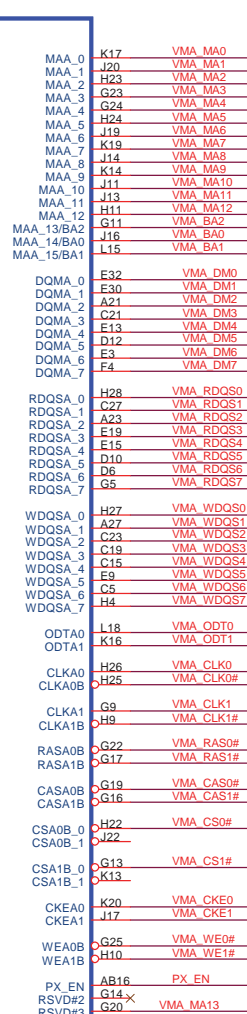


support 1Gbit  
VRAM ( 64M X 16 )

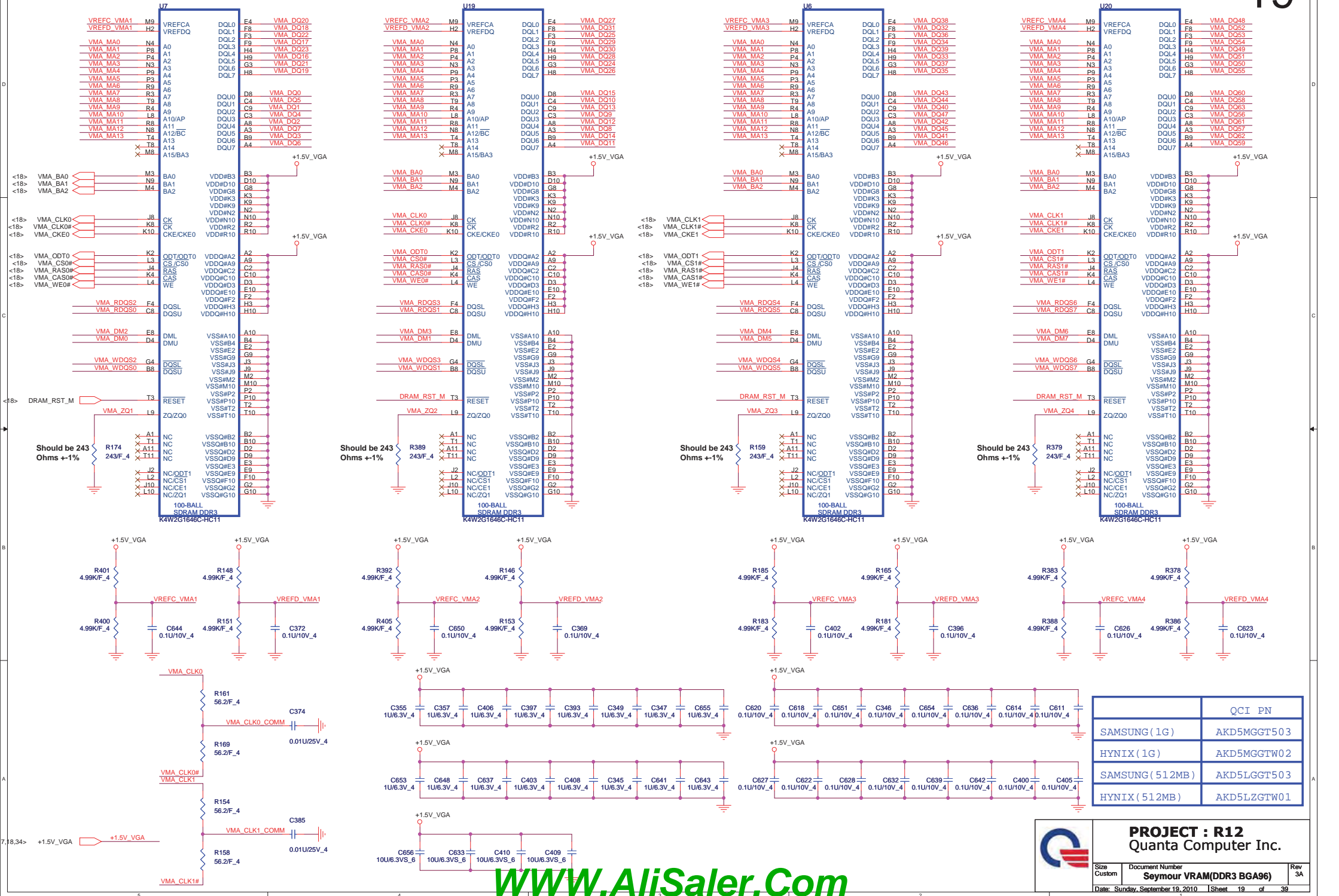
DIVIDER RESISTORS	GDDR5	DDR3
MVREF TO 1.8V (Ra)	40.2R	40.2R
MVREF TO GND (Rb)	100R	100R

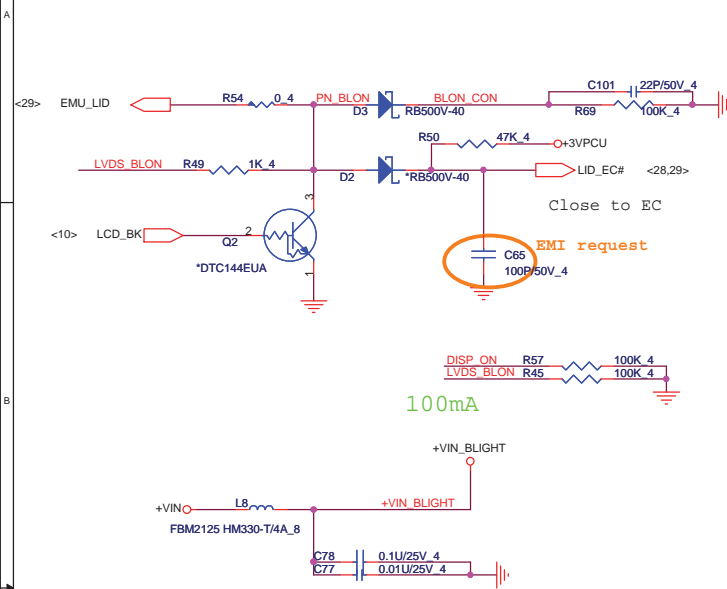


MEMORY INTERFACE

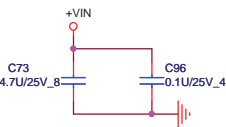




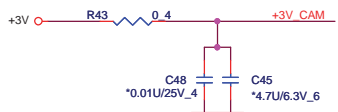
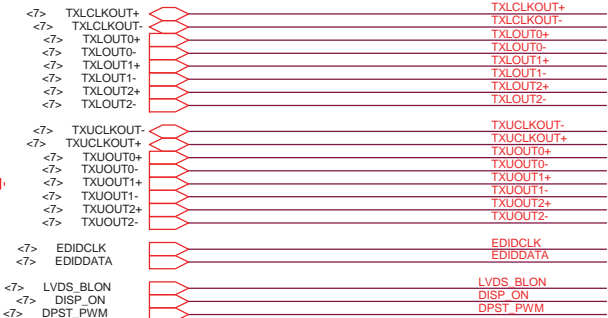
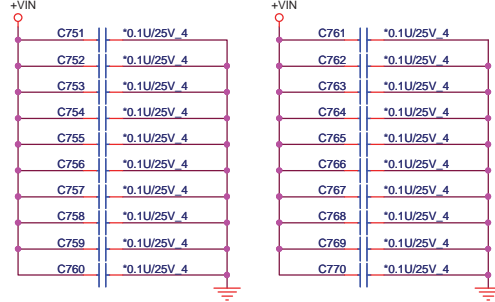




EMI & RF

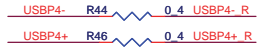


Coupling CAP.

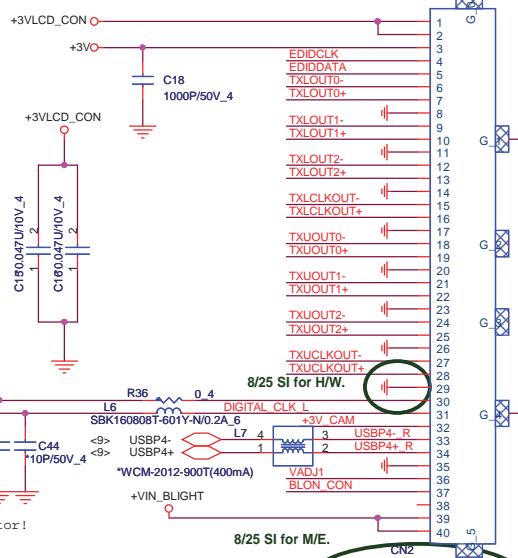
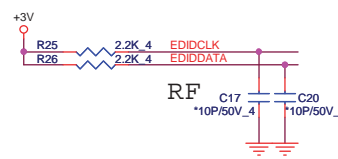
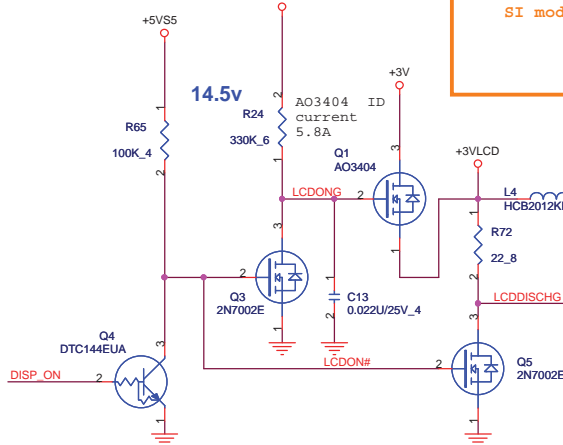


Please note that 2011 camera is +3v a We do not need to use 5V -> 3.95V regulator!

follow L4 location



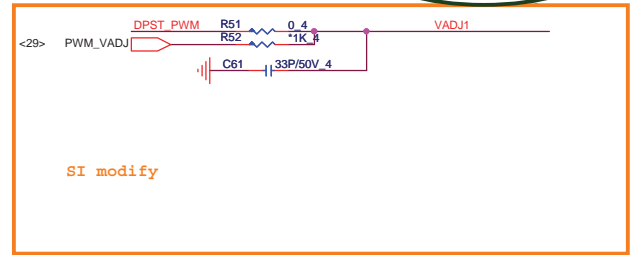
change to +5VS5



EMI

8/25 SI for H/W.

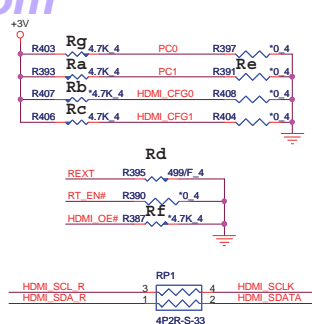
8/25 SI for M/E.



PROJECT : R12  
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LCD CONN/LID/CAM	1A
Date:	Sunday, September 19, 2010	Sheet 20 of 39

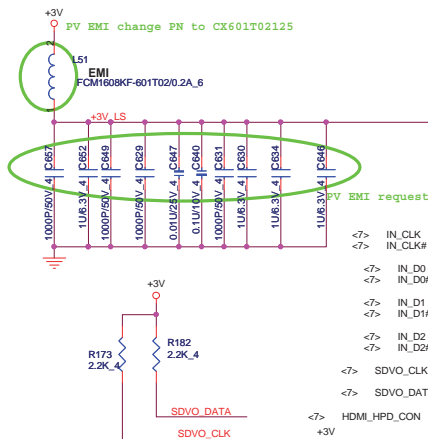
Signals		<i>PDT</i>	<i>PIM</i>	<i>CHR</i>
PC1	<b>Ra</b>	4.7K	4.7K	NC
HDMI_CFG0	<b>Rb</b>	NC	NC	NC
HDMI_CFG1	<b>Rc</b>	4.7K	NC	NC
REXT	<b>Rd</b>	499	4.7K	1.2K
PC1	<b>Re</b>	NC	NC	4.7K
HDMI_OE#	<b>Rf</b>	NC	NC	4.7K
PC0	<b>Rg</b>	4.7K	4.7K	4.7K



Vendor	Part	Part Number	Part Description
PDT	PSB101	AL008101000	IC OTHER(48P) PS8101QFN48GTR(QFN)
PIM	PI3VDP411LSRZBE	ALP411LS004	IC OTHER(48P) PI3VDP411LSRZBE(TQFN)
CHR	CH7318C	AL007138002	IC OTHER(48P) CH7318C-BF-TR(QFN)

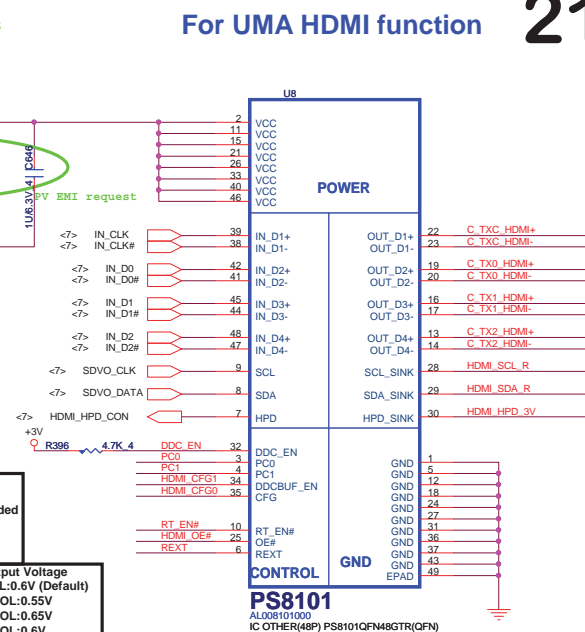
9/16 : PIM: need use ALP411LS000 or ALP411LS004 for capella

CHR : need Na R1182, add R1027 for capella



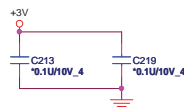
EQUALIZATION SETTING	
PC1:PC0=0:0	8dB
PC1:PC0=0:1	4dB Recommended
PC1:PC0=1:0	12dB
PC1:PC0=1:1	0dB

**SCLZ/SDAZ Low-level input/output Voltage**  
 CFG1:CFG0=0:0 VIL:<0.4V VOL:0.6V (Default)  
 CGF1:CGF0=0:1 VIL:<0.36V VOL:0.55V  
 CGF1:CGF0=1:0 VIL:<0.44V VOL:0.65V  
 CGF1:CGF0=1:1 VIL:<0.36V VOL:0.6V

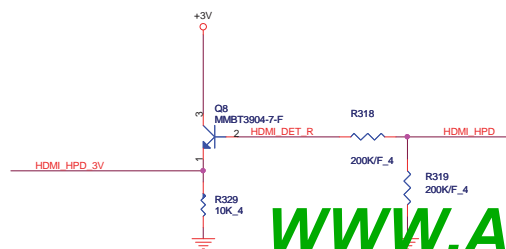
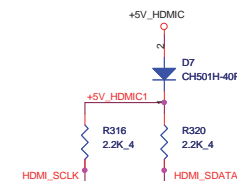
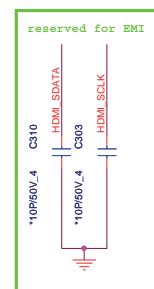
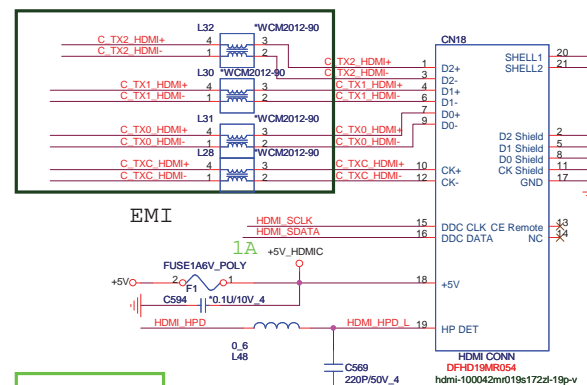


### For UMA HDMI function

21



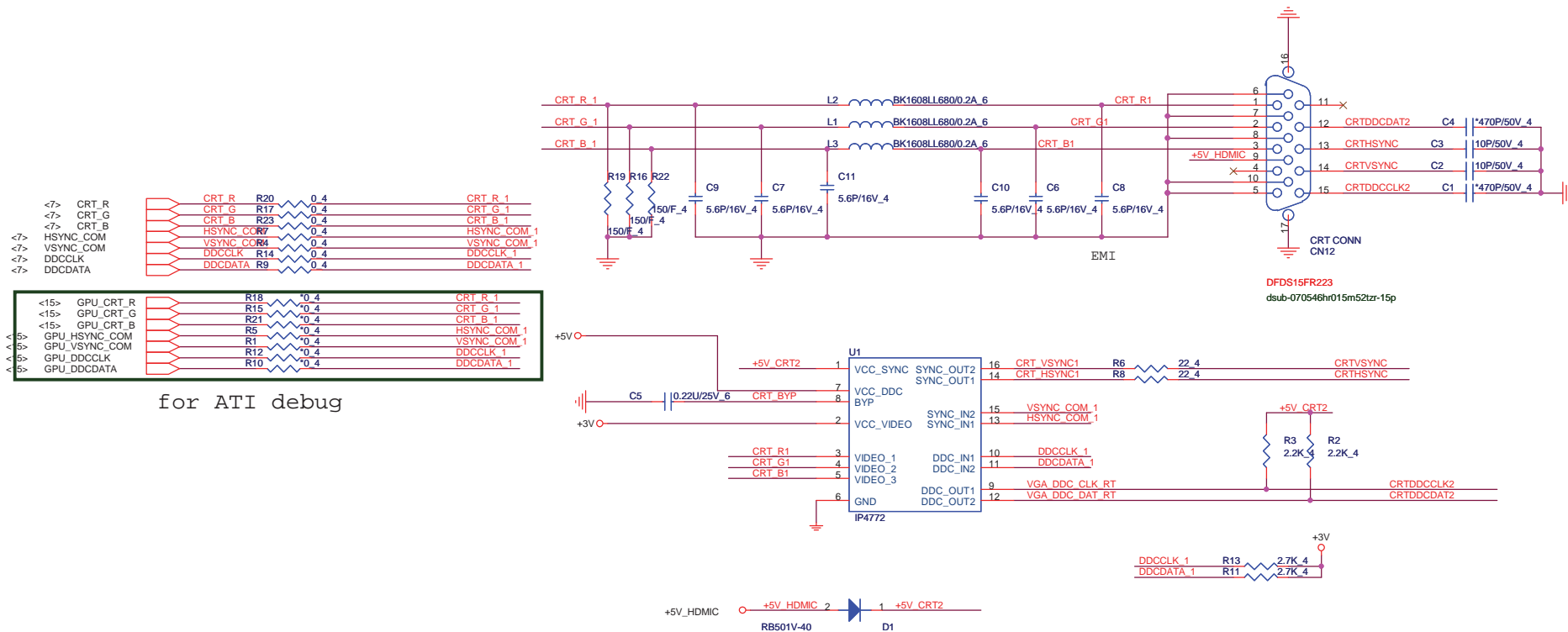
8/25 SI for EMI reserve.



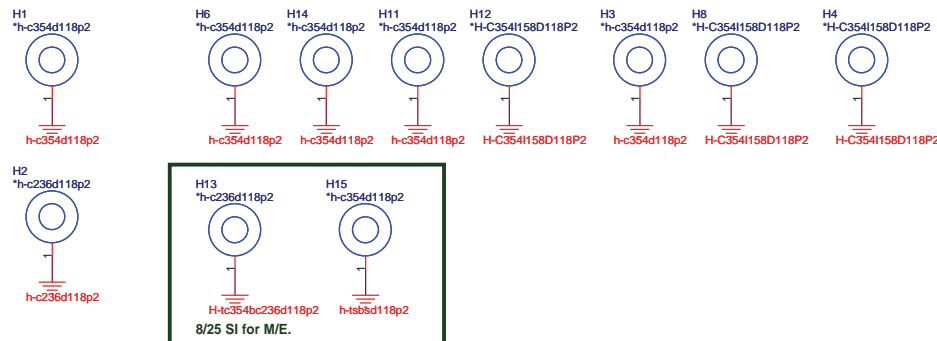
**PROJECT : R12**  
Quanta Computer Inc.

Size Custom	Document Number <b>HDMI CONN</b>	Rev 1A
Date: Sunday, September 19, 2010      Sheet 21 of 39		

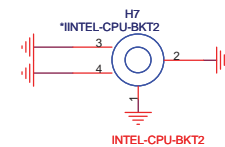
## CRT PORT



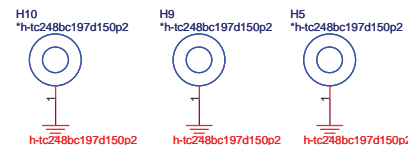
## HOLE



## CPU

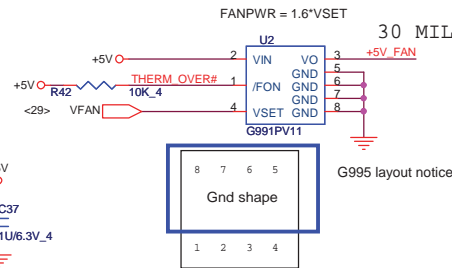
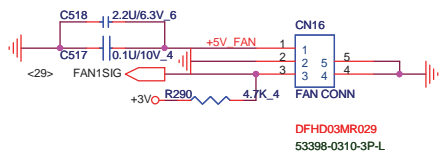


## VGA



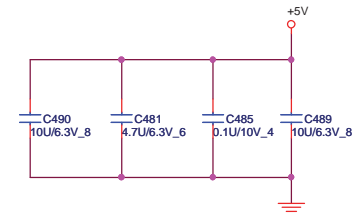
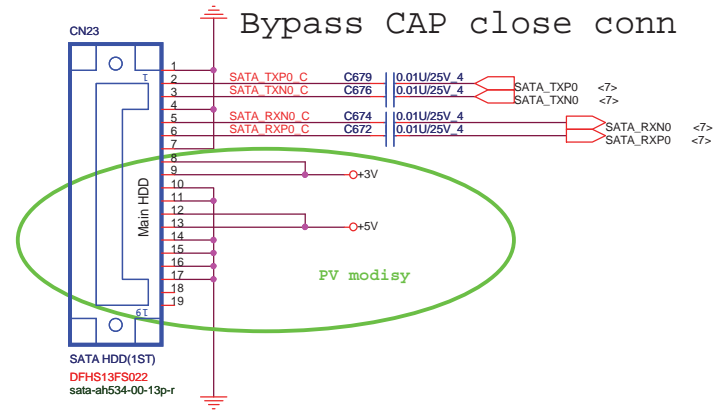
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Quanta Computer Inc.

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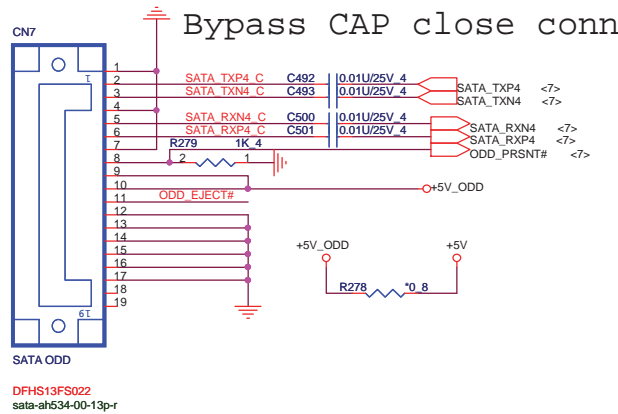


## SATA HDD CONNECTOR

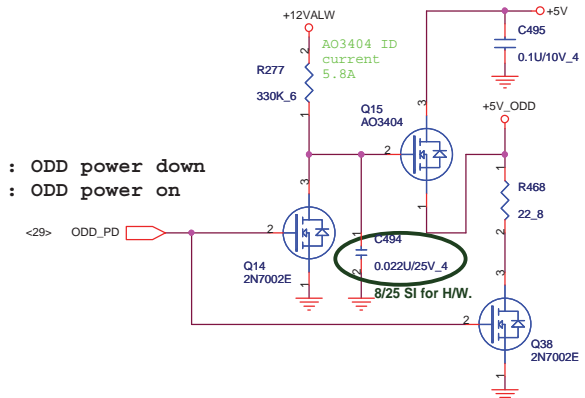
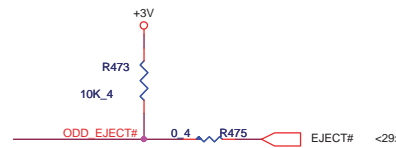
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## SATA ODD CONNECTOR



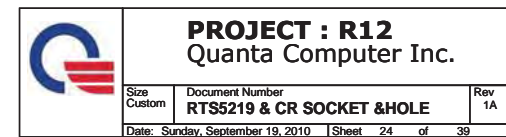
High : ODD power down  
Low : ODD power on

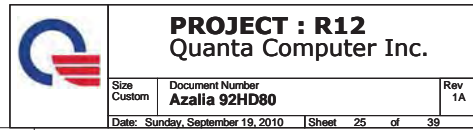


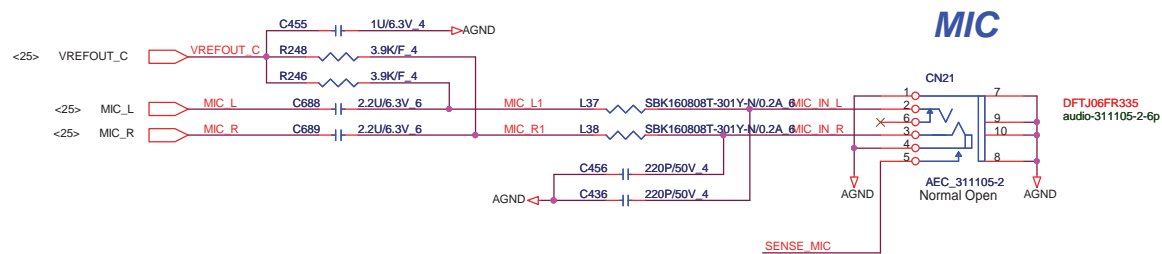
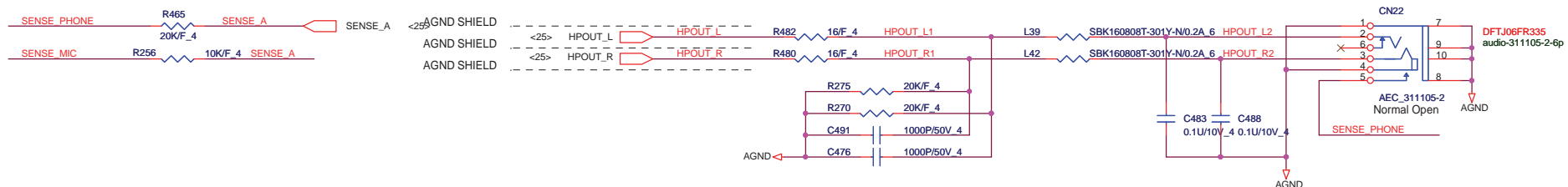
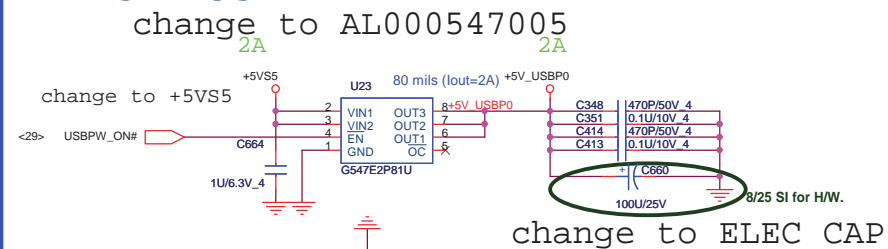
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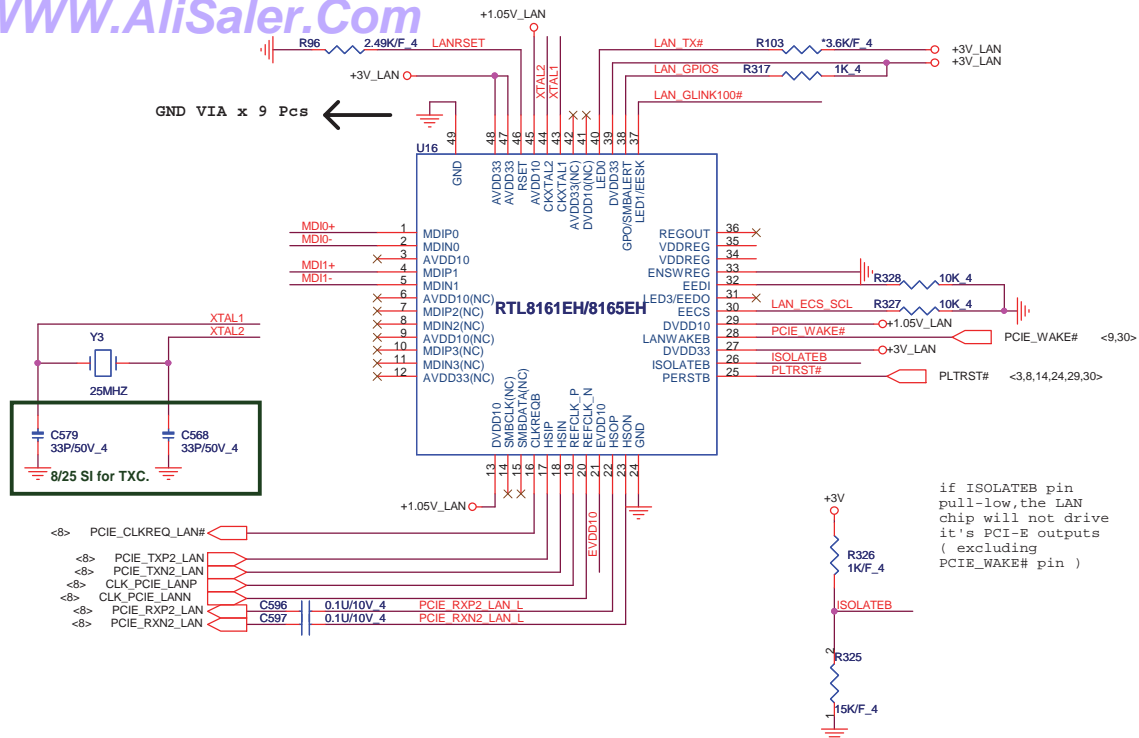
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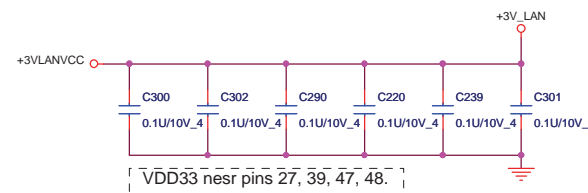
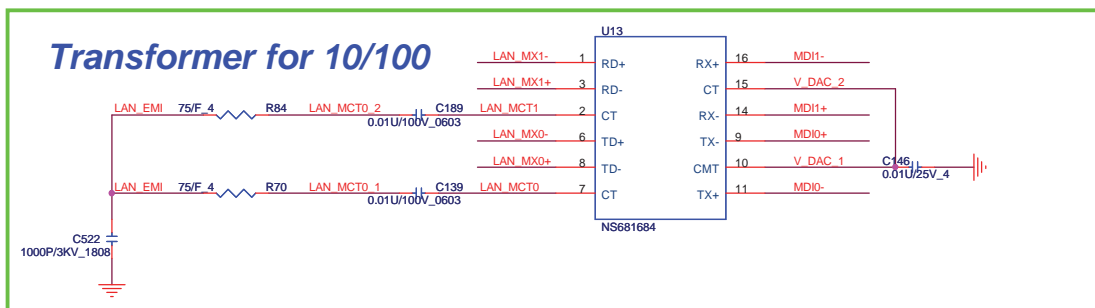
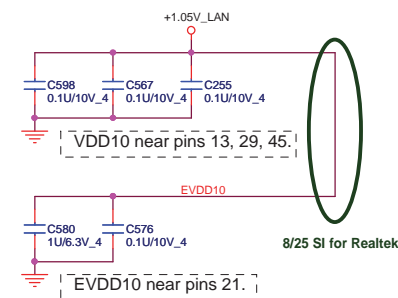




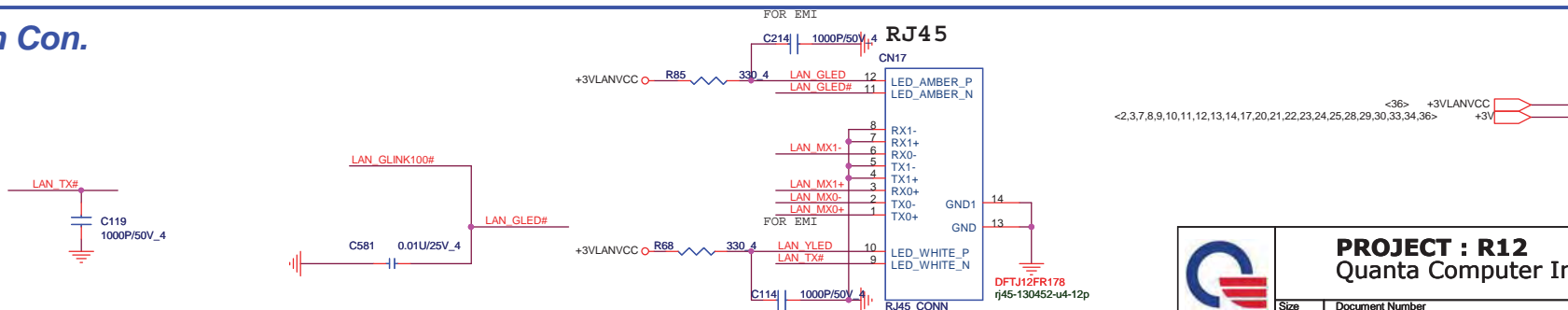




Power trace Layout 寬度 > 60mil  
> 60mil

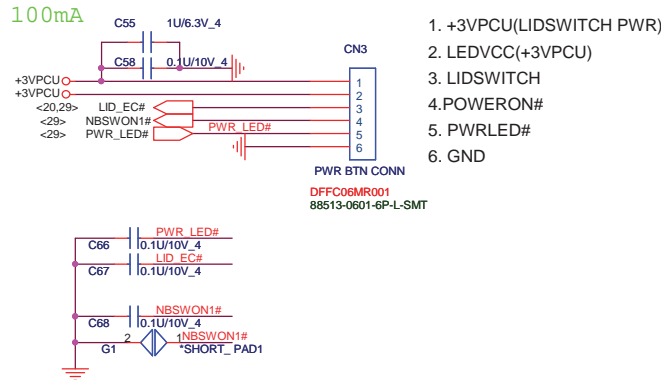


## Lan Con.

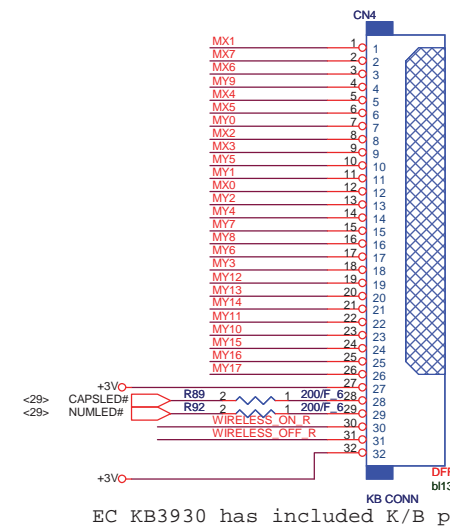
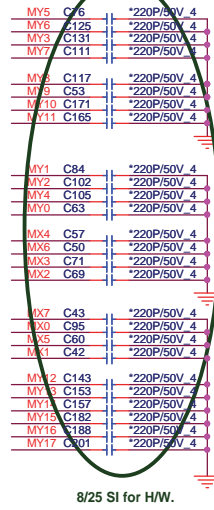


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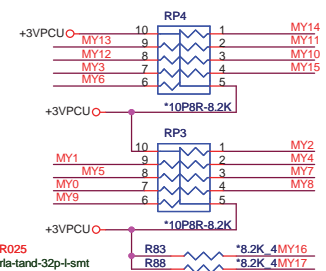
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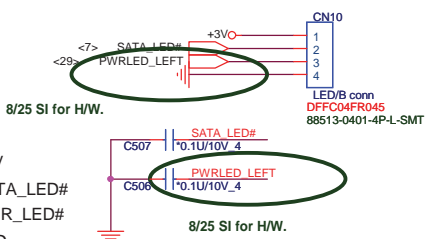
## KEYBOARD Con.



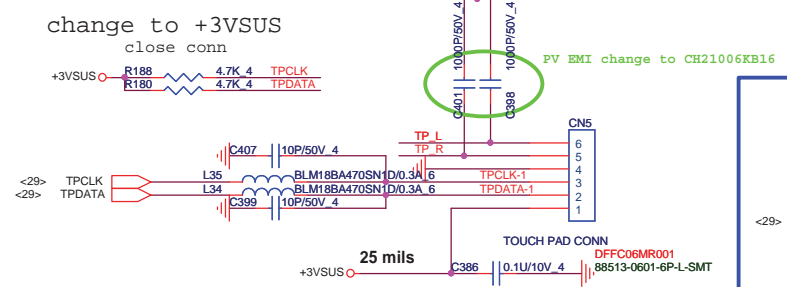
## KEYBOARD PULL-UP



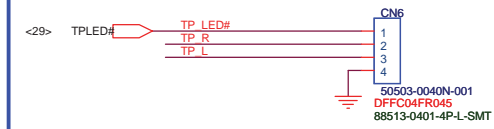
## LED Con.



## TOUCH PAD Con.



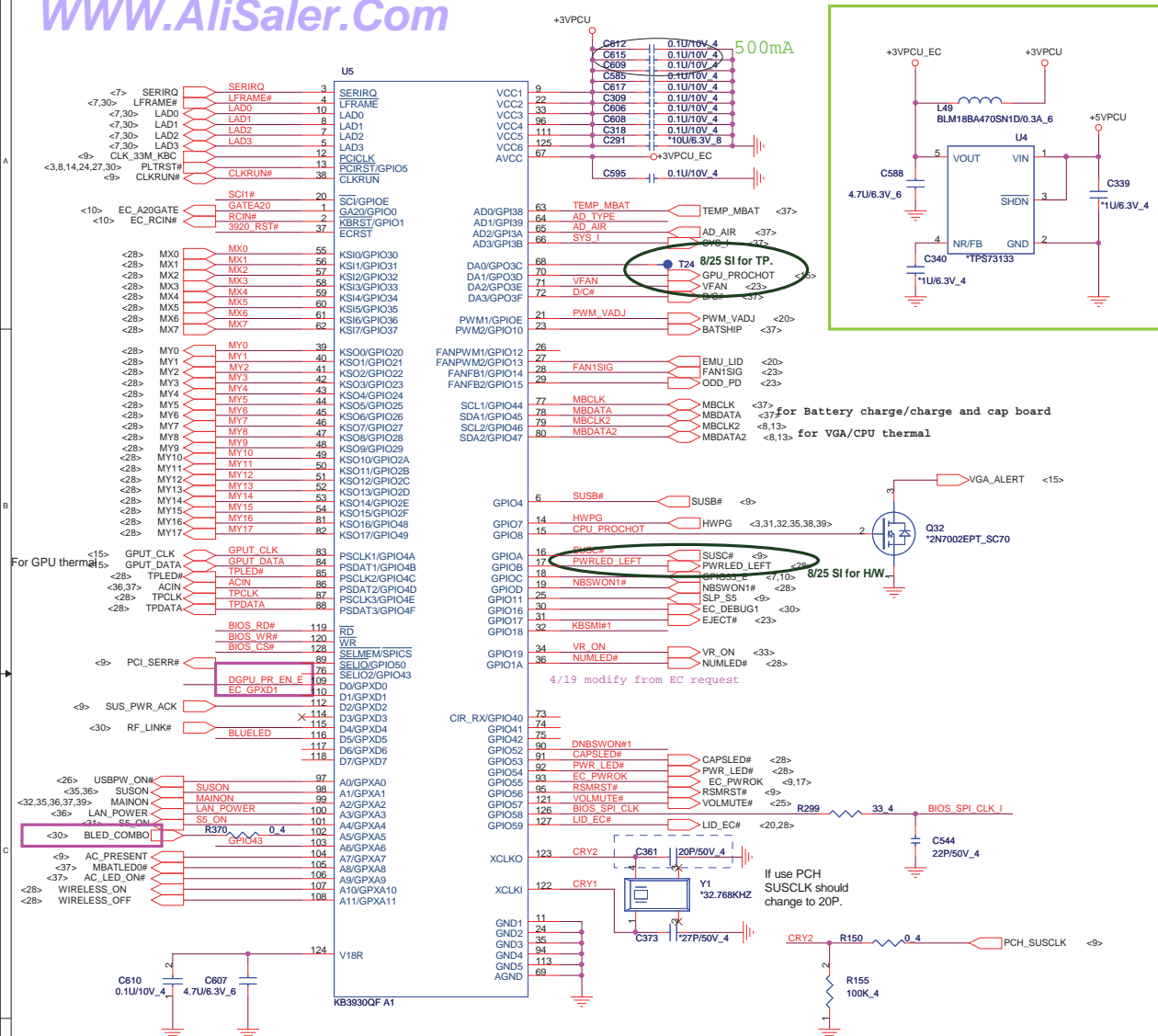
## To TOUCH PAD SW board



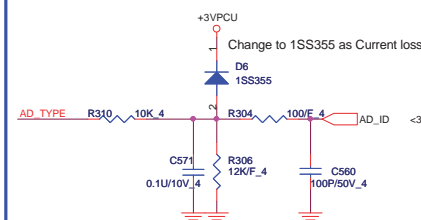
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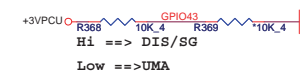




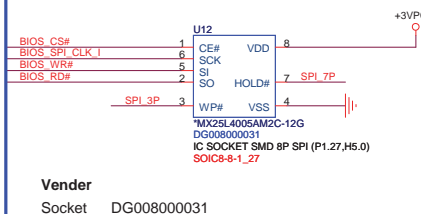
## adapter Type check



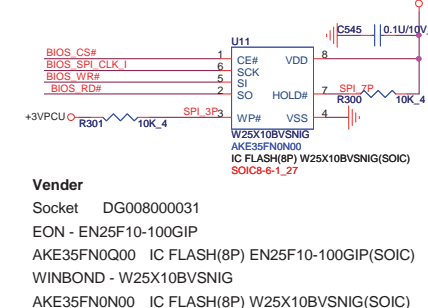
## adapter select for EC



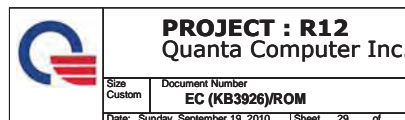
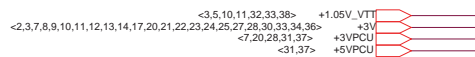
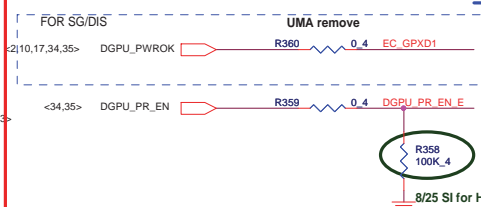
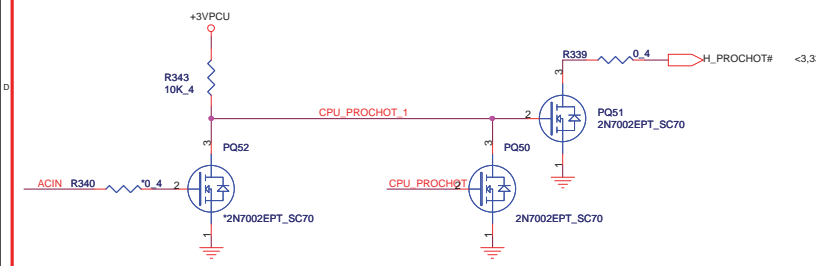
## 512K byte SPI EC ROM



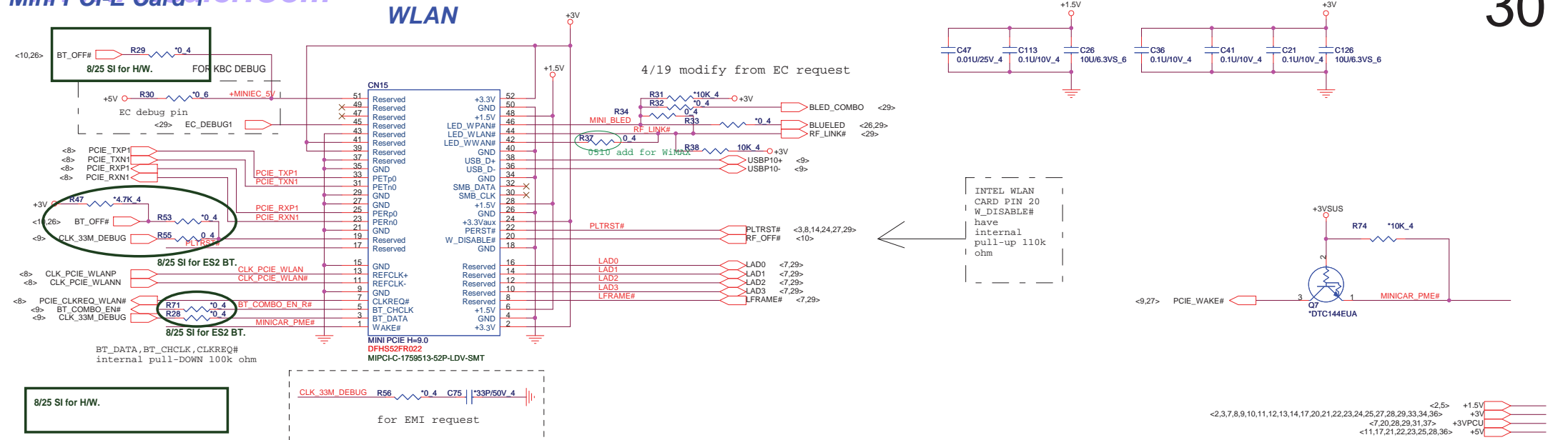
## 128K byte SPI EC ROM

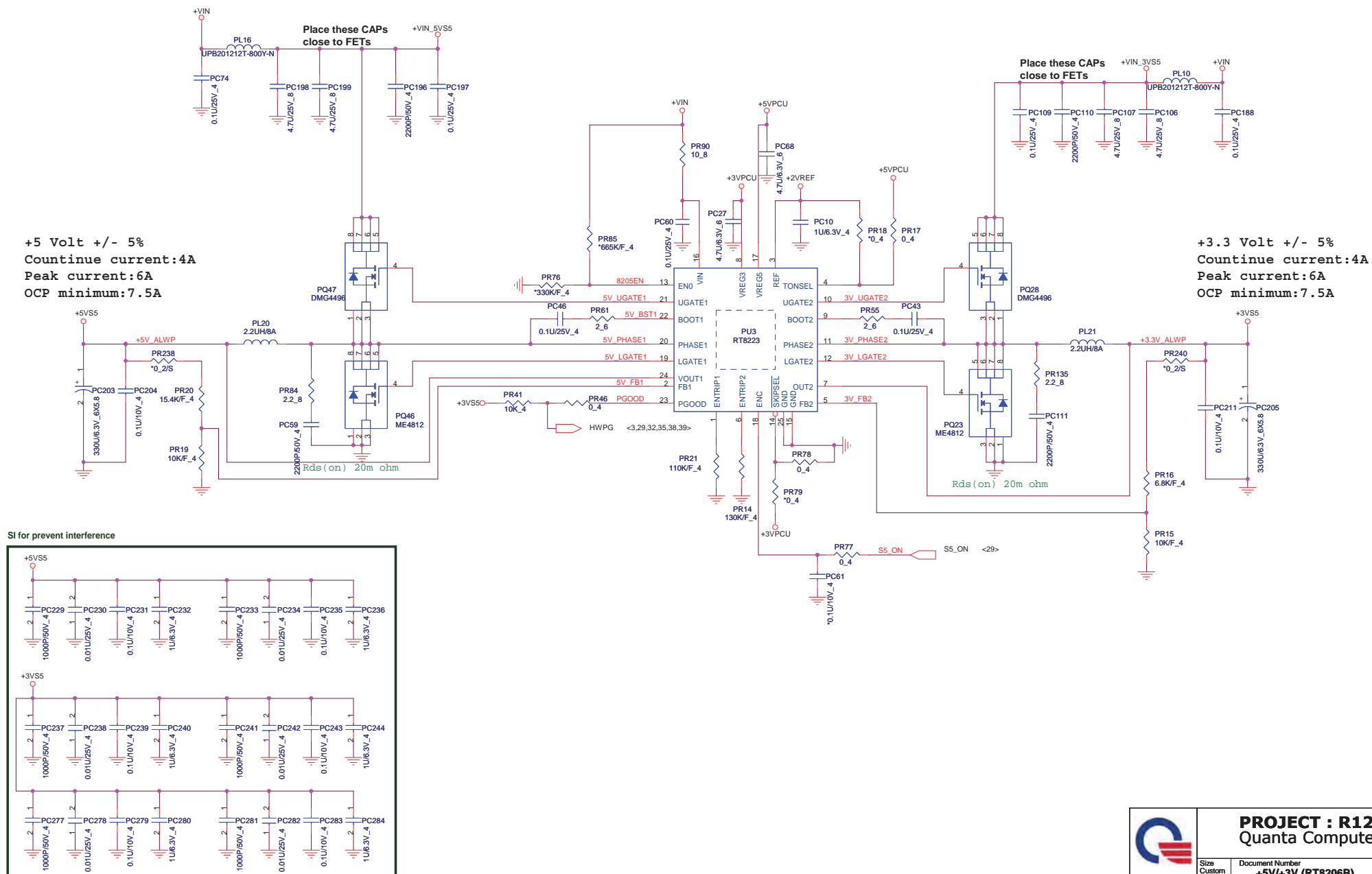


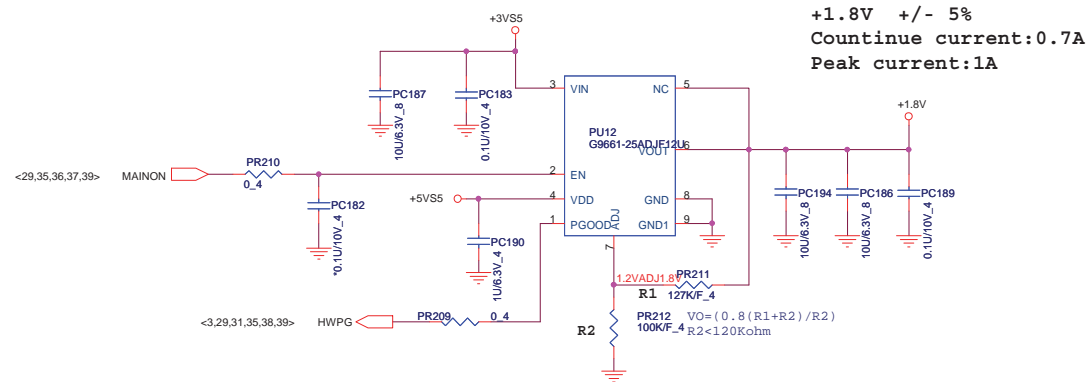
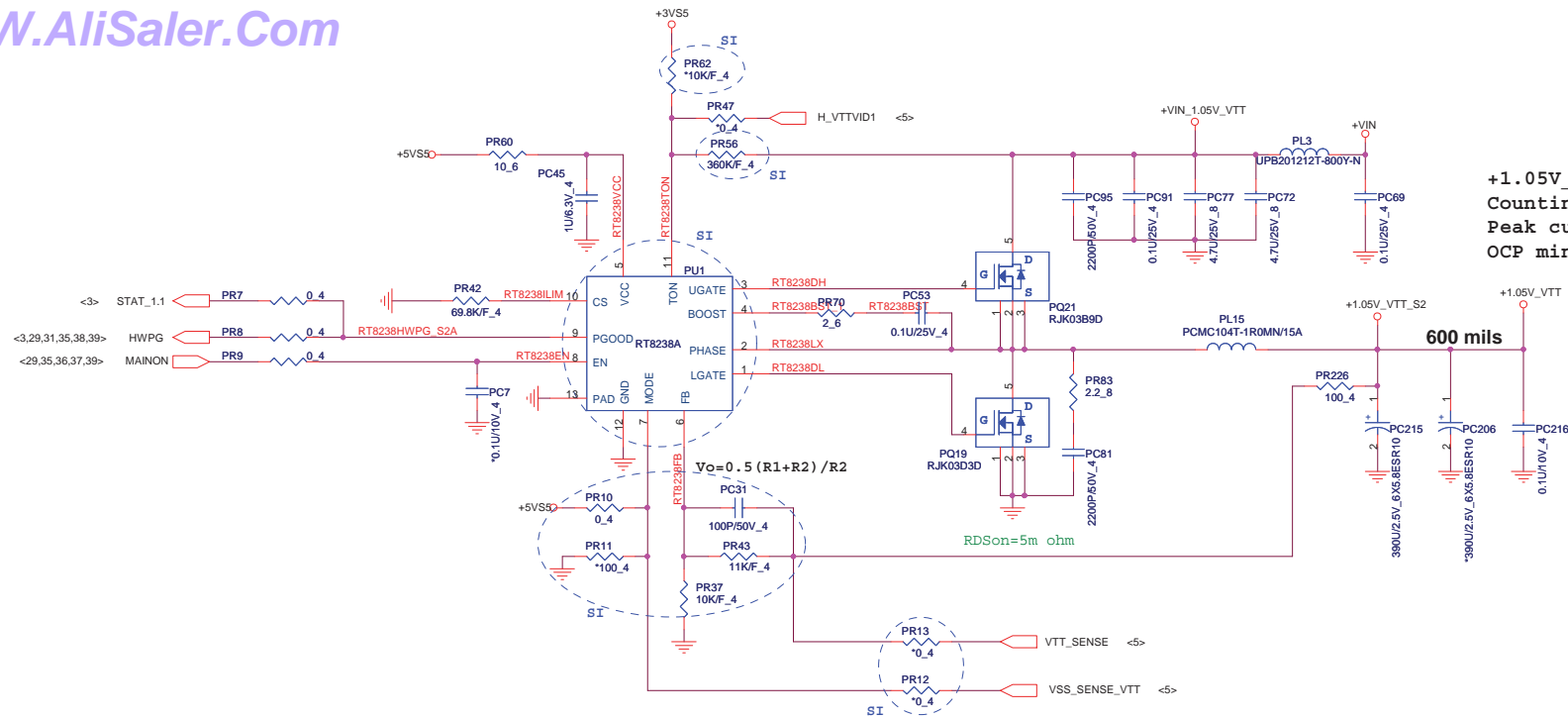
AC present: AC\_IN-->high, CPU\_PROCHOT-->low, H\_PROCHOT#-->high  
Remove AC: AC\_IN-->low, CPU\_PROCHOT-->low, H\_PROCHOT#-->low  
Remove AC and re-cove prochot: AC\_IN-->low, CPU\_PROCHOT--> high, H\_PROCHOT#--> high




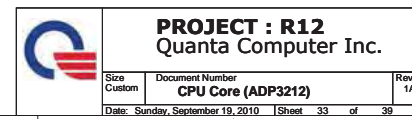
# WLAN



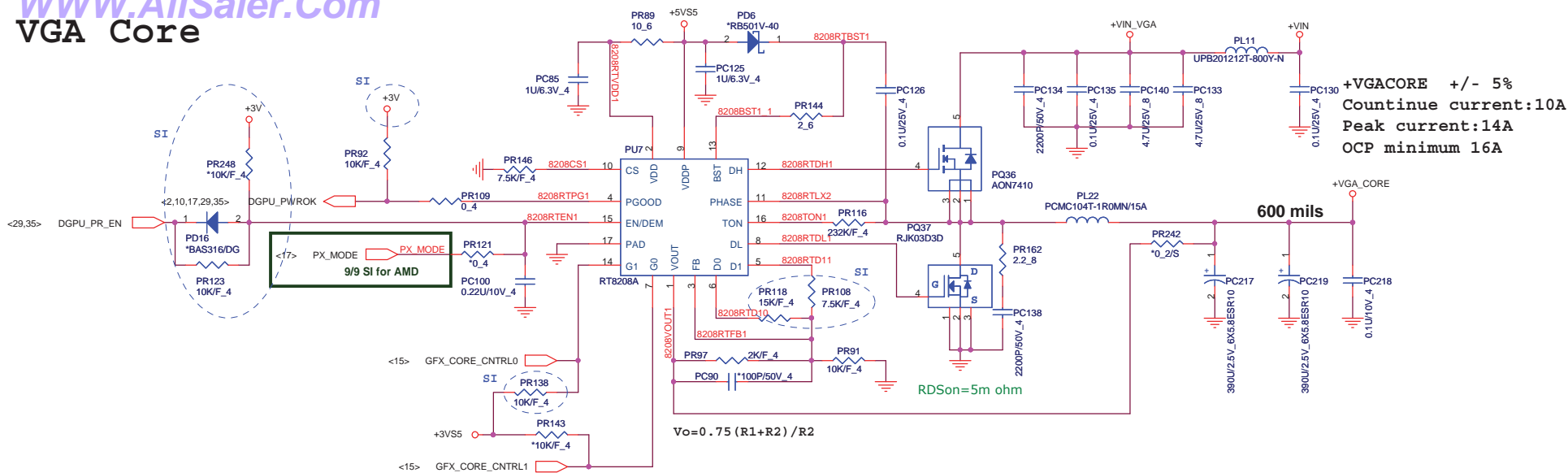




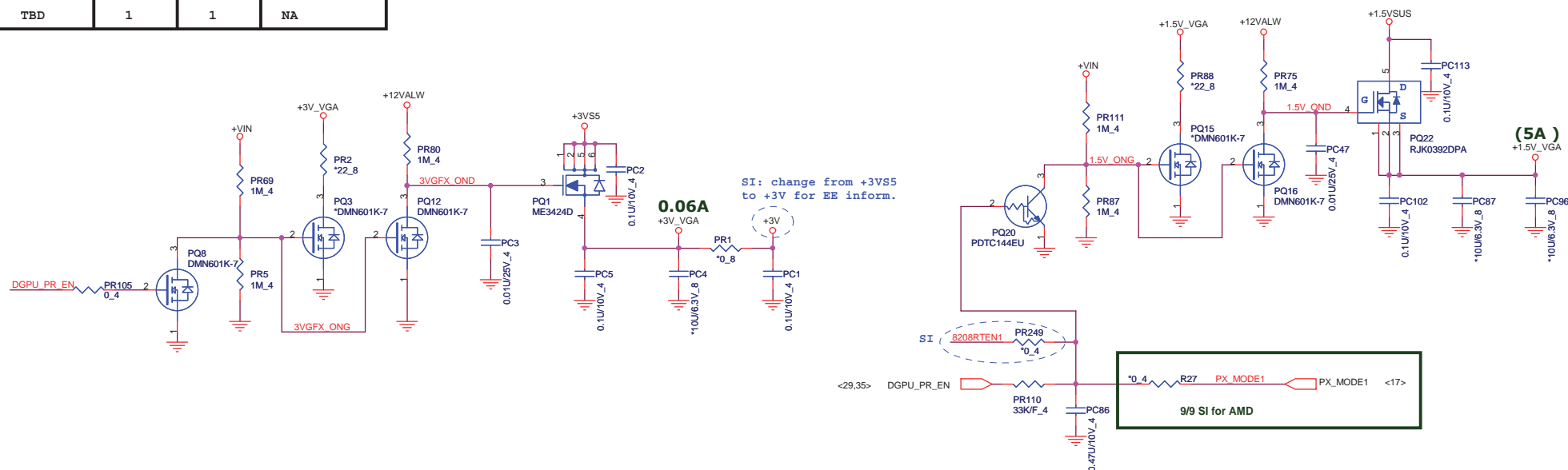
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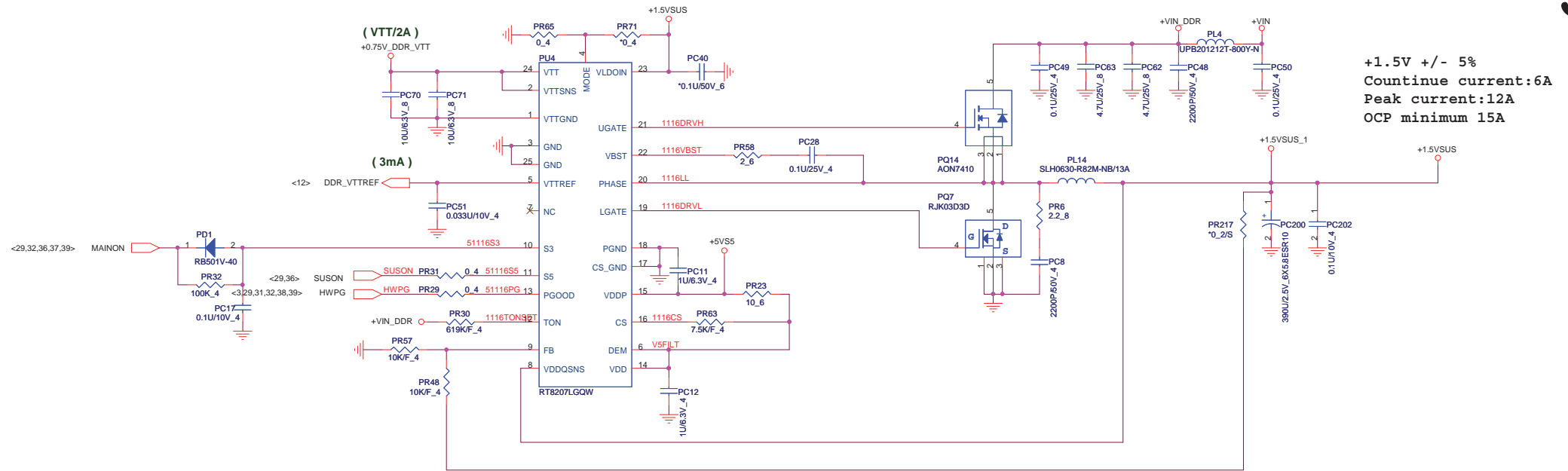




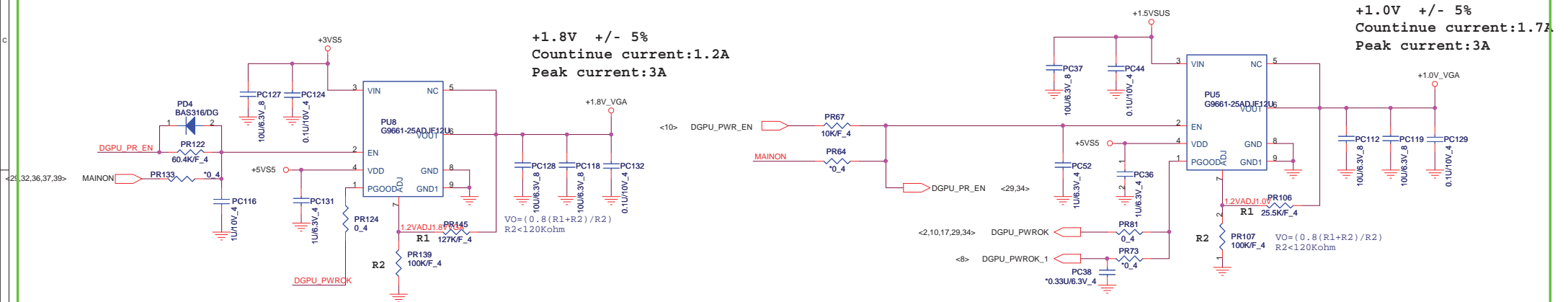


Seymour-XT	PWRCNTL0	PWRCNTL1	V-CORE
L	0	0	0.9V
M	0	1	1V
H	1	0	1.1V (Default)
TBD	1	1	NA



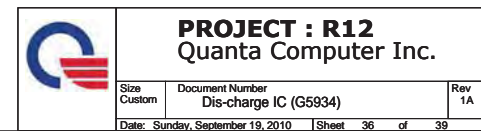


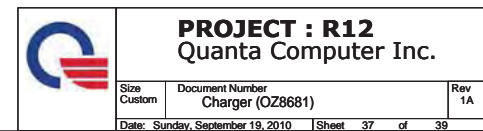
## SG &amp; Discrete Only



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